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Analysis of Total Harmonic Distortion and Voltage Performances of Reduced Multi-level Inverter with Photovoltaic Systems

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ABSTRACT: -Multilevel inverter is used in various applications that need high voltage and high current. The topologies of multilevel inverterhave several advantages such as lower total harmonic distortion (THD), lower electromagnetic interference (EMI) generation, highoutput voltage. The main feature of multilevel inverter is the ability to reduce the voltage stress on each power device due to theutilization of multilevel on the DC bus. The advent of multilevel inverter topologies has caused variety of pulse widthmodulation strategies. In this paper, a new approach of MLI is proposed with reduced count of semiconductors for operations with SPWM modulation technique, which can minimize thetotal harmonic distortion and enhances the output voltages from seven and fifteen level inverted voltage waveforms.The proposed MLI with SPWM is able to generateoutput voltage fromPV system as source, which reducestotal harmonic distortion (THD) in comparison to conventional inverter. Major harmonic components in output voltage are less in magnitude when proposed MLI with PWM technique is applied to inverter. Fundamental component of output voltage is also higher in proposed PWM method for all modulation index and frequency ratio. Performance of proposed topology has been evaluated by MATLAB/simulation for single phase 7- level and 15-level MLI for both symmetrical and asymmetrical modes.

Keywords:SPWM, Multilevel inverter, THD.

I. INTRODUCTION

A multilevel inverter is a power electronic interface thatsynthesizes a desired output voltage from several DC voltagesas inputs [1]. The research and development for these types ofconverters are gaining popularity especially for high power andhigh voltage applications due to the reduction in THD. Due tothis the size of the passive filter will be smaller making the overall system compact. In addition to this, it produces outputwaveforms with a better harmonic spectrum, hence improvedpower quality and also has good electro-magneticcompatibility. Conventional multilevel inverters include diodeclamped converter [2], flying capacitors [3], cascaded H-bridge
[4]. The cascaded H-bridge and the diode clamped are the most
popularly hardware implemented topologies at present,especially in the growing technological field of renewableenergy.

Multilevel inverters have some disadvantages. One of themost obvious disadvantages is the numerous of powersemiconductor switches required. Every switch requires a gatedriver circuit, therefore increasing the complexity and size ofthe overall circuit. The requirement of multiple gate drivercircuit leads to large expense, consequently in practicalapplications a reduction in the number of switches used iscrucial. This paper presents a new topology of a cascadedmultilevel inverter that has fewer semiconductor switches andgate driver circuits with higher number of steps in the output [5]-[7]. Amultilevel inverter with a lower THD by means of adopting appropriate PWM techniques would be beneficial for the design of a more compact passive filter.

II. REDUCED SWITCHES MLI

The Fig. 1 demonstrates the basic topology of multilevel inverter proposed in this paper. The multilevel converter consists of nine switches (IGBT) which gets energized by three sources neighboring them. The synthesized output from MLI can be achieved by providing different paths to the connected sources for conduction with help the of switching pattern of power switches [8]. A variation in values can be considered for the sources. Therefore, two sections, symmetrical and asymmetrical, are organized to illustrate the proposed structure. Modularity is the other important

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features of the proposed structure, so it can be used in high voltage applications [9]-[12].

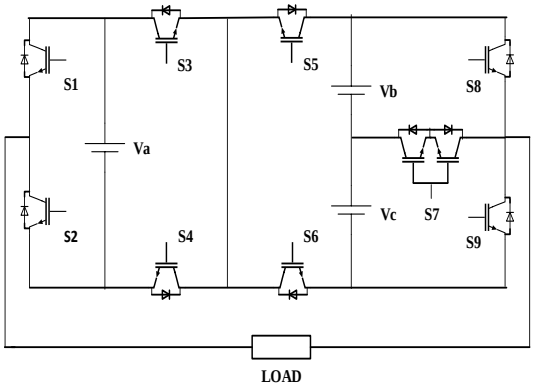

Fig. 1 Schematic view of proposed Multilevel Inverter

For symmetrical MLI topology, all the value of DC sources areequal in magnitude and energized by PV systems. The three voltage sources are V_a, V_b and V_c. Where $V_a = V_b = V_c = V_{dc}$ which correspond to different switching states summarized below. That by one or more switching states same voltage levels can be obtained. There are 4 switches working in each mode for generate a output voltage. The voltage level V_{dc}, for instance, can be produced by two sets of different redundant switching states. The redundancy of switching state is a common phenomenon in MLIs [13]. It provides a more flexibility for switching pattern designing also. Generalized 7-level output voltage waveform of symmetrical MLI is shown in fig. 10.

Mode-I: - Below fig. 2 shows the conduction path of symmetrical MLI in mode-I. To get the output voltage$V_{load} = 3V_{dc}$, 4 switches i.e., S_2, S_3, S_6 and S_8 is turned on. Thus, it involves all 3 DC sources (V_a, $V_b$andV_c) having equal magnitude of voltage (V_{dc}) & load and completes the path for current conduction. Hence $3V_{dc}$ output voltage obtained across the load.

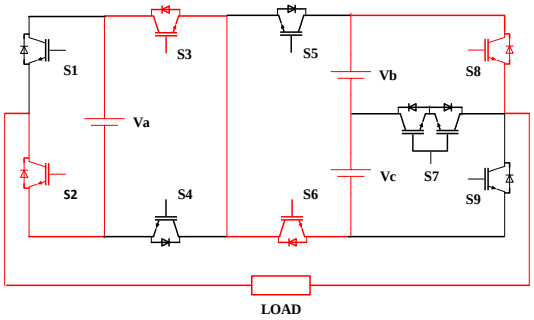

Fig. 2 Mode-I of 7-level symmetrical MLI; $\mathbf{V_{load}} = \mathbf{3V_{dc}}$

Mode-II: - Below fig. 3 shows the conduction path of symmetrical MLI in mode-II. To get the output voltage$V_{load} = 2V_{dc}$, 4 switches i.e., S_2, S_3, S_6 and S_7 is turned on. Thus, it involves 2 DC sources ($V_a$andV_c) having equal magnitude of voltage (V_{dc}) & load and completes the path for current conduction. Hence $2V_{dc}$ output voltage obtained across the load.

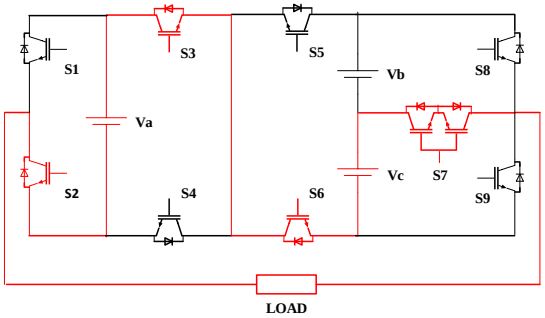

Fig. 3 Mode-II of 7-level symmetrical MLI; $\mathbf{V_{load}} = \mathbf{2V_{dc}}$

Mode-III: - Below fig. 4 shows the conduction path of symmetrical MLI in mode-III. To get the output voltage$V_{load} = V_{dc}$, 4 switches i.e., S_2, S_3, S_5 and S_8 is turned on. Thus, it involves only one DC source (V_a) & load and completes the path for current conduction. Hence V_{dc} output voltage obtained across the load.

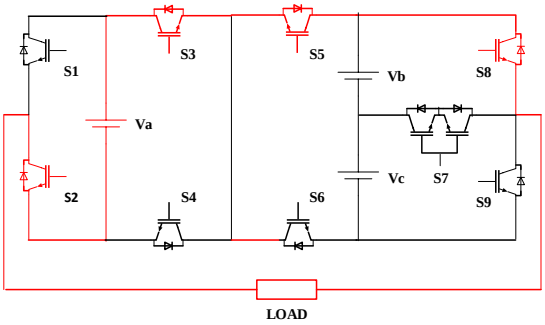

Fig.4 Mode- III of 7-level symmetrical MLI; $\mathbf{V_{load}} = \mathbf{V_{dc}}$

Mode-IV: - The conduction path for the 0-level output voltage is shown in red line in fig. 5 when switches S_1, S_3, S_5 and S_8 are turned ON. Thus, it involves none of DC sources.in this mode all sources are bypassed. Hence 0V, 0-level output voltage obtained across the load.

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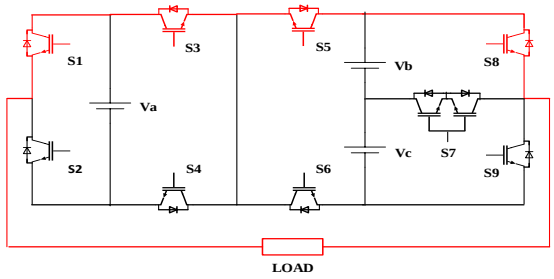

Fig. 5 Mode-IV of 7-level symmetrical MLI; $\mathbf{V_{load}}$ = 0

Mode-V: - Below fig. 6 shows the conduction path of symmetrical MLI in mode-V. To get the output voltageV_{load} = $-V_{dc}$, 4 switches i.e., S_1, S_4, S_6 and S_9 is turned on. Thus, it involves only one DC source (V_a) & load and completes the path for current conduction. Hence Vdc output voltage obtained across the load.

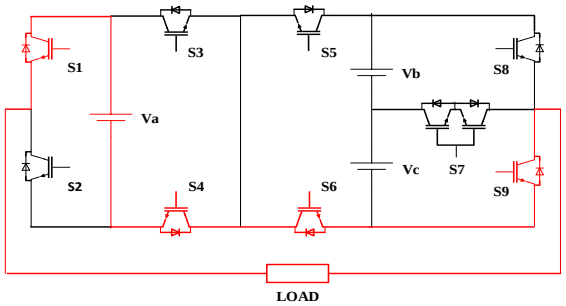

Fig. 6 Mode-V of 7-level symmetrical MLI; $\mathbf{V_{load}}$ = $\mathbf{-V_{dc}}$

Mode-VI: - Below fig. 7 shows the conduction path of symmetrical MLI in mode-VI. To get the output voltageV_{load} = $-2V_{dc}$, 4 switches i.e., S_1, S_4, S_5 and S_7 is turned on. Thus, it involves 2 DC sources (V_a and V_b) of voltage (V_{dc}) & load and completes the path for current conduction. Hence $-V_{dc}$ output voltage obtained across the load.

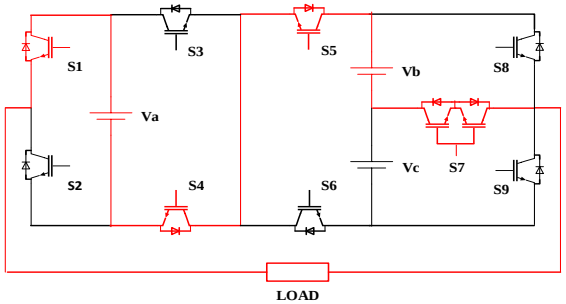

Fig. 7 Mode- VI of 7-level symmetrical MLI; $\mathbf{V_{load}}$ = $\mathbf{-2V_{dc}}$

Mode-VII: - Below fig. 8 shows the conduction path of symmetrical MLI in mode-VII. To get the output voltageV_{load} = $-3V_{dc}$, 4 switches i.e., S_1, S_4, S_5 and S_9 is turned on. Thus, it involves all 3 DC sources (V_a, V_b and V_c) having equal magnitude of voltage (V_{dc}) & load and completes the path for current conduction. Hence $-3V_{dc}$ output voltage obtained across the load.

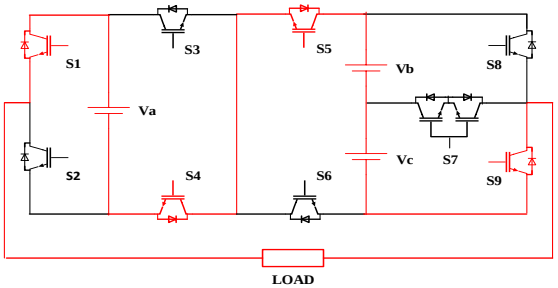

Fig.8 Mode-VII of 7-level symmetrical MLI; $\mathbf{V_{load}}$ = $\mathbf{-3V_{dc}}$

III. SWITCHING STRATEGY

There are many proposed modulation methods for operating multilevel inverter as depicted in below Fig. 4[14]-[17]The converter which use to ease low frequency or fundamental component for switching one or two commutation of power electronic elements for one period of cycle of output waveforms resulting in a staircase shape. The class of multilevel inverters using this strategy are called as SHE-MLI and SVC-MLI.

The most popular switching method in industrial applications implementation is the classic carrierbased Sinusoidal PWM (SPWM) which uses the phase-shifting technique to decrease the harmonic content in the output load voltage [18]-[20]. The SVM strategy is one of another, which has also in use by other multi-level inverters.

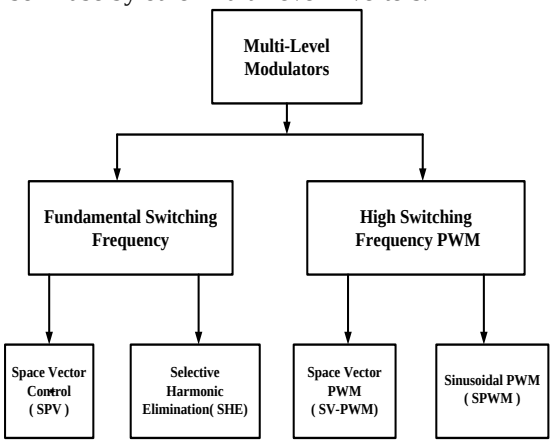

Fig. 9. Schematic view of proposed Multilevel Inverter

There are various types of SPWM techniques which are classified depending on carrier signal frequency, amplitude and phase. They are divided as follows [21]-[23];

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i. Phase Disposition PWM (PD-PWM)
ii. Phase Opposition Disposition PWM (POD-PWM)
iii. Alternative Phase Opposition Disposition PWM (APOD-PWM)
iv. Phase Shift PWM (PS-PWM)
v. Carrier Overlapping PWM (CO-PWM)
vi. Multi Carrier Sinusoidalwith Variable Frequency Pulse Width Modulation (MCVF-PWM)

The switching methodology implemented in this paper mainly deals with control sequence of power electronic switches in the MLI which shows its effect in the output parameters of proposed MLI. The paper shows the use of multi-carrier frequency compared with sinusoidal modulating waveform. The mainrole of a carrier based PWM technique is the comparison of a sinusoidal waveform with a carrier waveform, which is basically being a triangular carrier waveform. The reference signal is continuously compared with the carrier signal [24]. The instant where reference is greater than the carrier signal, then the switch corresponding to that carrier gets activated or de-activated [26].

The switching strategy used for operation of proposed topology for MLI consist of two patterns i.e., symmetrical and asymmetrical. The above proposed figure in Fig. 1 can be operated in two stages, generalized output waveform from proposed MLI in Fig. 5 and 6 respectively.

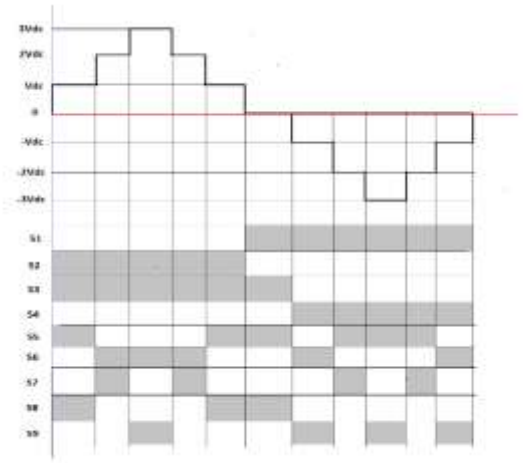

Fig. 10 Generalized Step waveform of 7-level MLI for one cycle.

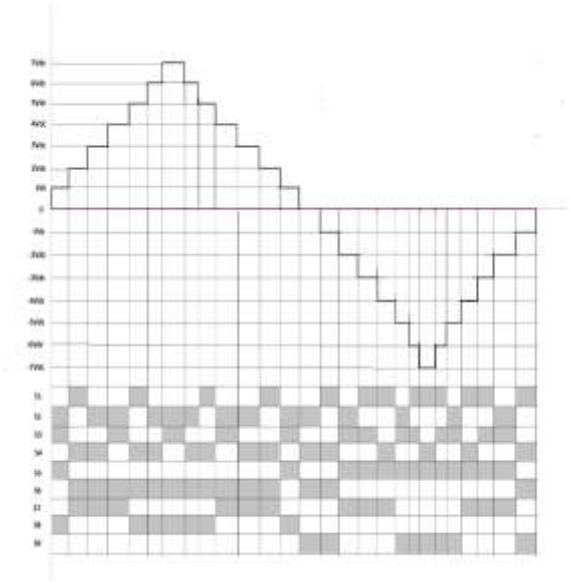

Fig. 11 Generalized Step waveform of 15-level MLI for one cycle.

The Fig. 12 and 13 shows the SPWM technique for above stated strategy for both fed by PVsources for mentioned MLI topology. It is possible to obtain voltage levels figured in Table I and II by suitably firing the switches in the as shown in below figure for the seven and fifteen level multilevel inverter. The firing pulses are generated using multicarrier pulse width modulation technique. For implementing this technique, as shown in Fig.12 and 13, a standard sinusoidal wave is compared with 14 levels of triangular wave to generate the firing pulses for each switch in the stated multilevel inverter. A conventional SPWM with triangular carriers canexplained an ‘n’ Level MLI, (n-1) carriersare required [27]-[30].

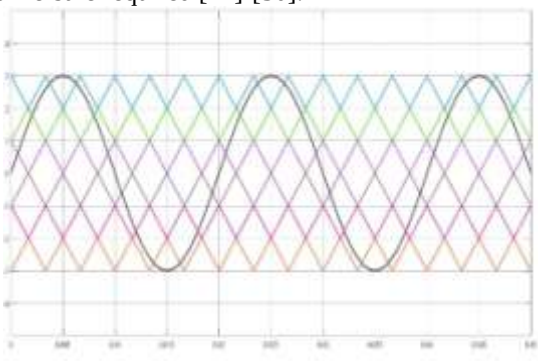

Fig. 12 Multicarrier SPWM for proposed 7-level MLI.

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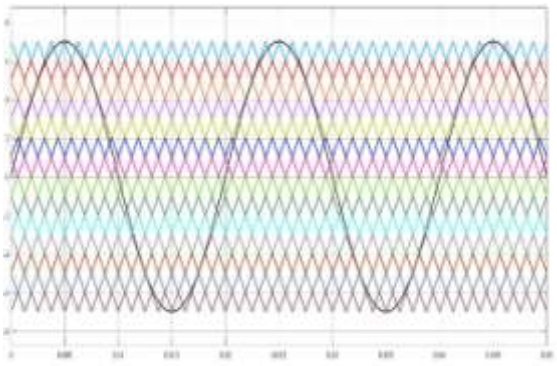

Fig. 13 Multicarrier SPWM for proposed 15-level MLI.

IV. SIMULATION RESULTS

In this section. IV, the verification operation of the proposed topology isconducted, it is simulated for different output voltage levelsin MATLAB/Simulink environment for symmetric and asymmetric modes. The simulation study has been carried for a series R-L ac load for both schemes (where, R= 100 Ω and L= 10 mH) to create 50 Hz single phase sinusoidal voltage and current waveform.

A. The Proposed 7-level Symmetrical topology

In this scheme, the proposed topology with symmetrical structure the values are $V_1=V_2=V_3=$ 100V PVsource and the switched as per states shown in fig. 10 and simulated. Fig. 14 and 15shows the output voltage and currentmentioned 7-level structure. The obtained results confirm the performance of the proposed topology. The THD value of output voltage based on simulation results is analyzed as 9.23% and depicted in fig. 16 and 17.

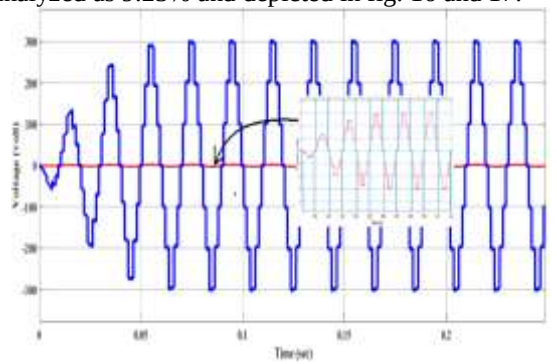

Fig. 14 Output voltage and current waveforms of 7-level MLI

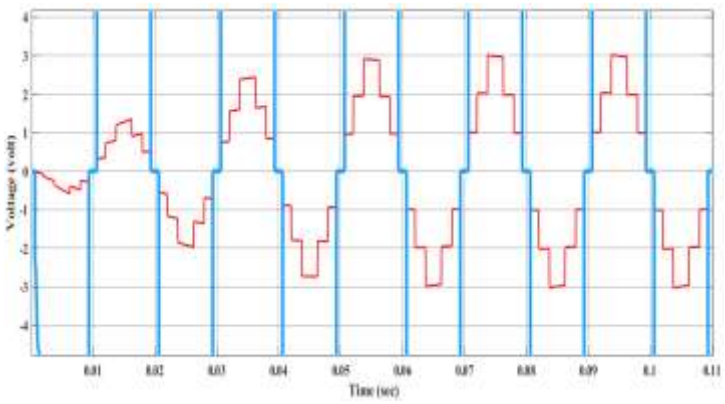

Fig. 15Zoomed view of current waveform achieving 7-level

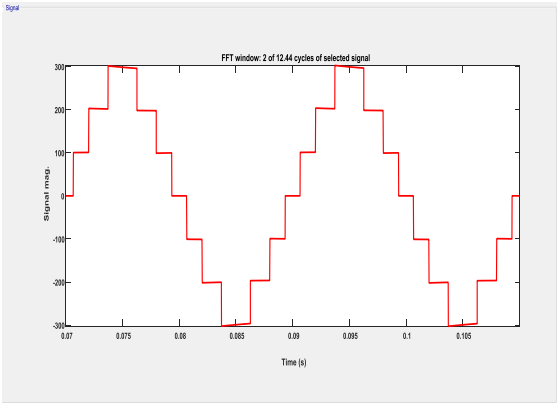

Fig. 16Highlighted two cycles for THD analysis for 7-lelvel MLI

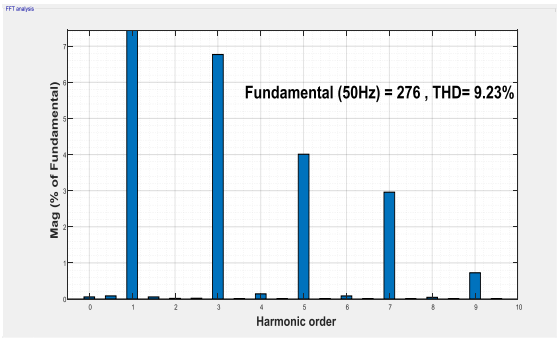

Fig. 17Harmonic spectral analysis of voltage for 7-level MLI.

B. The Proposed 15-level Asymmetrical topology

The same structure is stimulated for achieving higher level by replacing the equal PVsources with unequal in magnitudes i.e., V1=50V, V2=V3=150Vthat provides maximum 343V on the output side of inverter as shown in fig. 18 and 19.The results are satisfactory and also quite similar to each other, which validates the performance of theproposed structure. The THD value of output voltage based on simulation is5.08% can be visualized in fig. 20 and 21.

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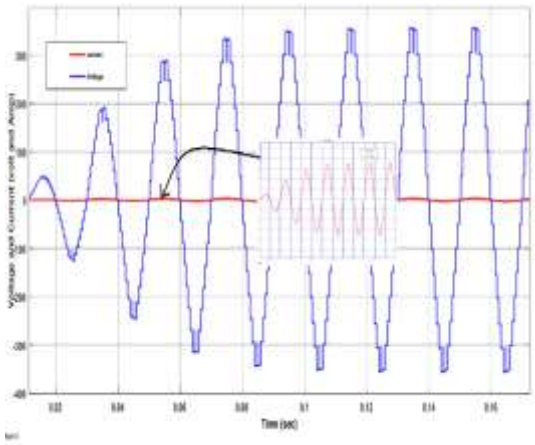

Fig. 18 Output voltage and current waveforms of 15-level MLI

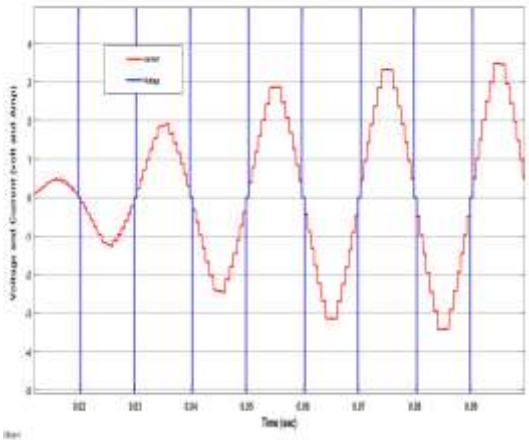

Fig. 19 Zoomed view of current waveform achieving 15-level

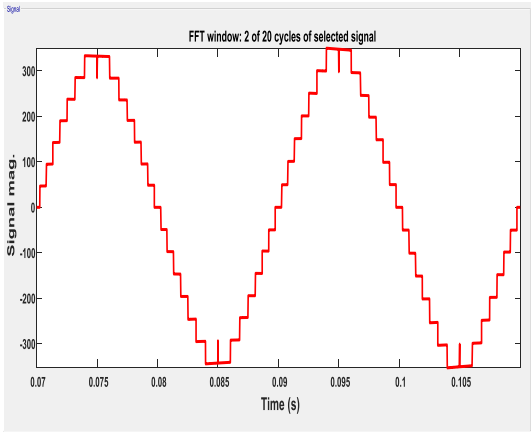

Fig. 20Highlighted two cycles for THD analysis for 15-lelvel MLI

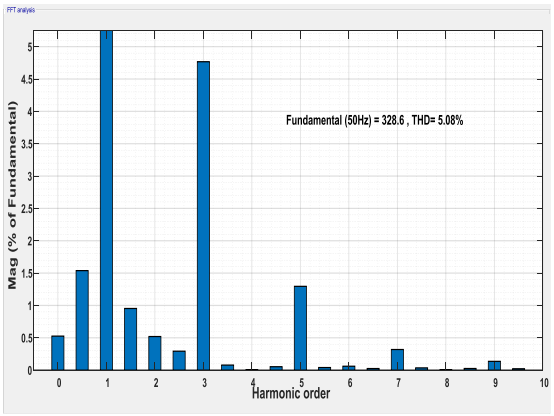

Fig. 21 Harmonic spectral analysis of voltage for 15-level MLI.

The below shown comparative analytic data in Table I depicts that as level of output waveforms of MLI increases, the efficiency and level get improved.

TABLE I. COMPARISON OF SYMMETRICAL AND ASYMMETRICAL MODES

Proposed MLI	**Output Voltage**	**Settling Time (run time is 1sec)**	**THD values for fundamental frequency**	**Efficiency of MLI**
Symmetrical Mode	295.6 Volts	0.14 secs	9.23%	86 %
Asymmetrical Mode	343.7 volts	0.06 secs	5.08%	93%

V. CONCLUSION

This paper concludes that proposed approach of MLI with lesser switches and PV as input to energize the circuit gives better synthesized output. With modification in input values in sources to MLI, the topology can be considered in both symmetrical and asymmetrical. The above analysis shows that when the degree of levelness increases, the rate of adaptivity in terms of response and efficiency also changes efficiently. The higher level of MLI possesses lower content of THD values as stated in above sections. The results for both cases in symmetrical and asymmetrical cases verifies the validity of proposed approach in MALTAB/Simulink environment.

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