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Design of QC LDPC Code Encoder using Dual Diagonal Matrix

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ABSTRACT—This paper presents an efficient encoding method and a high-throughput low-complexity encoder architecture for quasi-cyclic low-density parity-check (QC-LDPC) codes using dual diagonal matrix. Low Density Parity Check (LDPC) codes are one of the block coding techniques that can approach the Shannon's limit within a fraction of a decibel for high block lengths. These constructed codes are simulated to make the performance evaluation. The key interest of this research work was to inspect the performance of LDPC codes.

Keywords: quasi-cyclic LDPC code; Shannon's limit; encoding

I. INTRODUCTION

In 1948, Claude E. Shannon demonstrated in his paper [1] that data can be transmitted up to full capacity of the channel and free of errors by using specific coding schemes. In 1962, Robert Gallager proposed the new coding technique, Low Density Parity Check (LDPC) codes. For executing these codes, a huge measure of figuring power is required because of high intricacy and prerequisites of memory for encoding/unraveling tasks. So, for almost thirty years the work done by Gallager was ignored until in 1996, David Mackay introduced turbo codes.

D.Mackay showed that LDPC codes could approach The Shannon's limit. When perfectly decoded using iterative decoding techniques LDPC codes does remarkable performance near Shannon's limit.

LDPC codes are a linear block code and are most widely used types of forward error correction codes in digitalcommunication system. It is perceived by a very sparse parity-check matrix. This implies that the parity-check matrix has an exceptionally low grouping of 1's in it. That's the reason why it is called as Low-Density Parity Check code. The sparseness of LDPC code is the trademark which can lead to great execution as far as in terms of bit error rates.

LDPC codes are the most favored sort of codes for viable applications in communication and storage system. It gives detection or rectification of the errors which happen in a correspondence through a noisy quantum channel. LDPC codes are known as practical class of classical error correcting codes because of its minimal representation and good execution, particularly for short code lengths. Its characterization is effectively testable for not just hypothetical use yet in addition for computer experiments. It provides high performance error-correction scheme. LDPC codes are promising contender for future generation wireless communication principles.

These codes can be obtained by a discrete mathematical characterization for module.

Gallager promulgate the presence of the class of LDPC codes but in any case, he didn't give the through how to generate the parity-check matrix. It is also called the 'H' matrix. There are numerous techniques proposed by different scientists for generation of parity-check matrix. Those methods incorporate:-

- Random generation subject to constraints
- Density Evolution
- Finite Geometry

These are various ways to examine parity-check matrix when generating it. It includes minimum distance, cycle length and linear independence.

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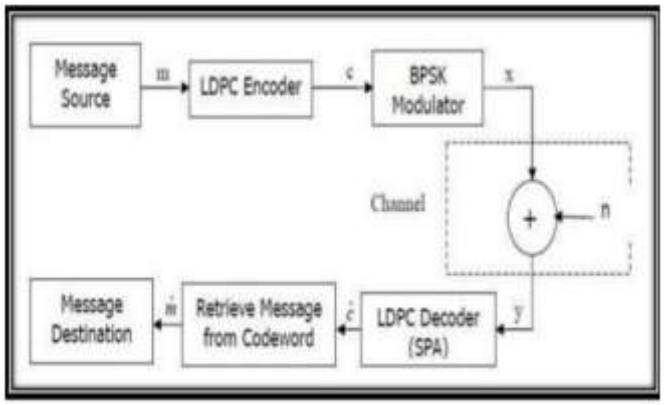

II. BACKGROUND

A. QC-LDPC CODES

The parity check matrix of QC-LDPC codes can be portrayed as a base parity check matrix. The digit of the base parity check is

Base Parity Check Matrix of QC-LDPC Codes

Code Rates	**1/2, 2/3, 3/4, 5/6**
Codeword Block Lengths	**648, 1296, 1944**
Sub-matrix Sizes Z	**27, 54, 81**

QC-LDPC Code Parameters

Matrix demonstrates the right cyclic shift values of the identity Z x Z square sub-Matrix. The dash '-' demonstrate the zero one. The QC-LDPC encoder needs to support 4 codes rate, i.e., 1/2, 2/3, 3/4 and 5/6, and 3 codeword block lengths, i.e., 648, 1296 and 1944. To support 3 codeword block lengths, sub-matrix sizes Z are characterized as 27, 54 and 81. 12 base parity check matrices are characterized to help 4 code rates and 3 codeword block lengths.

B. Linear Encoding Process

The base parity check matrix can be divided into the two sub matrices. Let H = [H1 H2] be the apportioned base parity check matrix, where H1 is an (N-M) x M sub matrix, and H2 is an (N-M) x (N-M) matrix. Let c = [m p] be a codeword block, where m and p demonstrate the data bit sequence and parity bit sequence respectively. From the property that the right codeword fulfils the parity check equation, the parity bit sequence p can be determined as follows,

$$H.C^T = H_{1.m}{}^T + H_{2.P}{}^T = 0,$$

$$P^T = H_2^{-1}.H_{1.m}{}^T$$

III. METHODOLOGY

Above all it's important to understand LDPC codes also, what is dual diagonal matrix.

Quasi-cyclic low density parity check codes are characterized by a sparse matrix. It has got

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a lot of consideration as a forward error correction code since they have astounding error correcting performance. QC-LDPC encoder gives high throughput and a viable rate. Small number of clock cycles must be acted in encoding process to accomplish high throughput. The LDPC encoders can uphold different code rates and codeword block lengths.

The LDPC encoder can give 3.34 Gbps throughput. For effective QC-LDPC encoder, it considers four kinds ofrotate-left-accumulator circuits. The arrangement of QC-LDPC code's parity check matrix is by ZxZ square sub matrices. Each sub matrix is a identity matrix with a cyclic shift or zero matrix. Data bit sequence is increased by the parity check matrix during an encoding process. In parity check matrix, ZxZ square sub matrix is duplicated to the one Zxl sub arrangement of the data bits. The argumentation can be executed by a cyclic shifter because of the cyclic shift property of the sub-matrix. Numerous cyclic shifters are needed to accomplish high throughput. This is the explanation why the plan of cyclic Shifter is a significant issue in QC-LDPC encoder.

Here, we propose a high throughput QC-LDPC encoder by embracing the double inclining network. In the light of double slanting lattice, we propose high throughput QC-LDPC encoder plan. The objective of the encoder configuration is to utilize a smaller number of rationale components. The proposed encoder is likewise rate feasible to help different code rates and codeword block lengths.

$$H = \begin{bmatrix} P_{0,0} & P_{0,1} & P_{0,2} & \cdots & P_{0,n_b-2} & P_{0,n_b-1} \\ P_{1,0} & P_{1,1} & P_{1,2} & \cdots & P_{1,n_b-2} & P_{1,n_b-1} \\ P_{2,0} & P_{2,1} & P_{2,2} & \cdots & P_{2,n_b-2} & P_{2,n_b-1} \\ \vdots & \vdots & \vdots & \cdots & \vdots & \vdots \\ P_{m_b-1,0} & P_{m_b-1,1} & P_{m_b-1,2} & \cdots & P_{m_b-1,n_b-2} & P_{m_b-1,n_b-1} \end{bmatrix}$$

The QC-LDPC codes are symmetric which are most recent and gives high throughput. It encodes a size k,s = (sO,sI,….,sk data block which is of l) T of size into a codeword vector c n,c = (sO,sI,…,sk-I)T, by adding n-k parity bits obtained so that it should fulfill the condition given below,

H . c = 0,
Where H is parity check matrix.

At that point the matrix H is divided into two region. Hs is the sub-matrix for region where systematic bits are increased and Hp addresses the region where parity part of codeword is multiplied to H matrix such an extent that,

H = [Hs Hp]

The parity of bit of matrix Hp can be further decayed into two sub matrices as
Where
0 is identity matrix |ZxZ with zero cyclic shift. Vector like sub matrix Hp is made out of weight-3 columns

hO is the cyclic shift at first row.

a. Encoding of LDPC Encoder
It includes two tasks :-

1. Construct a sparse parity-check matrix
2. Generate codeword using this matrix.

In encoding process, development of parity check matrix is very important. They assume essential part in the plan of LDPC encoder. We have utilized dual-diagonal parity check matrix for the LDPC encoder. The principle benefit of utilizing dual diagonal matrix is that it diminishes the intricacy in the interaction of calculation. In can address the intricate codes without any problem.

b. QC-LDPC codes with dual diagonal parity structure

QC-LDPC codes having long codes can be encoded with low complexity. Utilizing shift enrolls, the encoder of QC-LDPC codes can be carried out. In this execution encoding would be directly corresponding to the code length. The parity check matrix H can be divided into square sub-blocks of size ZxZ in QC-LDPC code. In it we take three sub-block measures as Z = 27, Z = 54, Z = 81. At that point i,j be ZxZ zero sub block or identity matrix l with change which is situated at I-th line and j-th segment with k occasions. Cyclic shift is 0<k<Z to one side. Parity check matrix H with fundamental sub-block matrices P, .mZxnZ is characterized as,

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Thus, matrix Hp turns into a dual-diagonal structure.

C. Encoding procedures for QC-LDPC codes

Because of high value for codeword length(n), LDPC coding presents computational overhead and consequently the increasing complexity during the process of encoding a LDPC encoder. LDPC computational overhead is proportional to m o r m. As n increases, the overhead increments fundamentally.

Richardson found the technique to beat this issue. The measure of calculation needed in encoding was decreased by this technique. Dual-diagonal parity structure has significantly diminished the encoding complexity so that computational overhead is proportional to n. We will contrast our proposed encoding plan with Richardson's plan.

D. Conventional efficient encoding scheme

Richardson, et al proposed the effective encoding plan in which H is expected as lower triangular structure. The parity check matrix H is in the structure,

$$H = \begin{pmatrix} A & B & T \\ C & D & E \end{pmatrix}$$

Where,
A = Z(m-1)xZ(n-m)
B = Z(m-1)xZ
T = (m-Z)x(m-z)
C = ZxZ(n-m)
D = ZxZ
E = ZxZ(m-1)

The sub matrices A and C relates to symmetric part Hs and under Hp sub matrices B, D,T, E comes. At that point vector hp becomes,
Hp = [B^T D^T]^T

T is the lower triangular with identity matrices along the diagonal and every one of the sub matrices are sparse.

The matrix H is summed up with vector c then we get the equation,

As+ Bpo + Tp1 = 0
(-ET_1A + C)s + (-ET_1B + D)Po = 0
Where,
-ET'"= Z x Z sub-block.

It is acquired by sub-block addition operation (for example I - I +I - I..... - I +I) which aggregates segments of sub-matrix A. Note that,
-ET -1B+D = I
Since addition of all sub-block matrices at weight-3 piece of matrix Hp recommended in guidelines, for example, [1] result just ZxZ character network I. Solving Equation prompts direct arrangement of equality vectors p0 and p1 Thus, every parity bit vectors can be actuated as,
p0 = (-ET-1A + C)s
Tp1= As + B0,
p0 is obtained through accumulation of input bits. For p0 to get p1, block accumulation done misusing dual-diagonal lower triangular matrix T.

IV. PROPOSED ENCODING SCHEME

In the proposed plan of Encoder, we have decreased the number of logic components. An encoder has different code rate. It could be 1/2,2/3,3/4,5/6. As we probably are aware code rate and code word is a significant piece of encoding. Figure appeared the following is the block diagram of LDPC encoder.

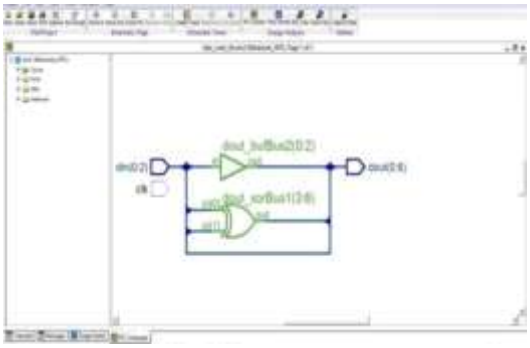

Diagram of Encoder

In our proposed LDPC encoder we have favor the code rate 5/6. It is liked to procure less region. Proposed encoder can utilize less region. Number of logic components utilized in the proposed encoder is lower than conventional encoder. The proposed encoder secures less complexity as age and estimation of the parity matrix is going on all the while. As both age and computation are going all the while, it saves time of calculation. The proposed encoder is likewise rate viable rather in customary encoder first moving is accomplished for creating the parity matrix then after parity calculationwas done and it procures a great deal of calculation time and builds the intricacy. It comprises of just two matrices in which one is diagonal matrix and other is cyclic shift which further partitioned in sub matrices. Sub-blocks are of 16x16. That is the reason it comprises 24 matrices in vertical direction and 120 matrices

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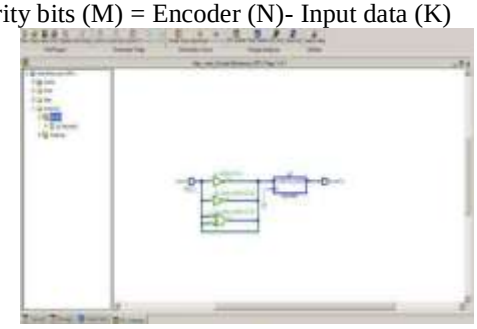
in horizontal direction. The computation done in the proposed encoder is block-wise so that we can utilize less registers and a smaller number of logic components. For the computation of circular shift matrix, we use rotator in the proposed encoder. So, calculation complexity will be less. Information utilized in the proposed QC-LDPC encoder is 120x16 bits. Input data(K) taken for the proposed encoder is 1920 bits. Encoder (N) is of 2304 bits. Consequently, we get the equality pieces of 384 bits.

Parity bits (M) = Encoder (N)- Input data (K)

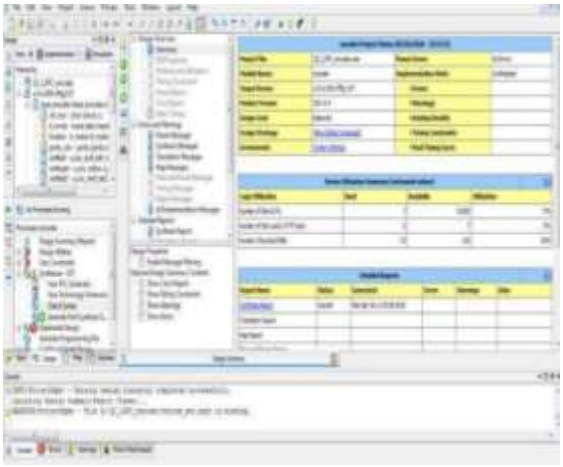


Schematic diagram of the encoder

Figure above is the schematic graph of the encoder. The codes are applied to produce the QC-LDPC codes. The quantity of LUTs utilized is 7 and time delay is 1.46ns. Cyclic shifter is utilized to lessen the complexity of the calculation. Results demonstrate that the proposed QC-LDPC Encoder is utilizing a smaller number of logic components and lessens the complexity of the calculations.

V. RESULT AND ANALYSIS

The proposed QC-LDPC encoder utilizes a smaller number of logic components and diminishes the complexity of the calculation. Calculation was done block wise, and this shows the outcome in lessening the quantity of logic components. In this proposed encoder creating of parity bits and computations are finished at the same time. This likewise saves time of calculation as both cycle is going on all the while. The figure appeared beneath shows the synopsis of the gadgets utilized in the planning of the QC-LDPC codes. Cyclic shifter is utilized to reduce the complexity of the calculation. Results demonstrate that the proposed QC-LDPC Encoder is utilizing a smaller number of logic components and reduces the complexity of the calculations. The codes are applied to create the QC-LDPC codes. The quantity of LUTs utilized is 7 and time delay is 1.46ns.



Summary of device used

Parameters	Base	Proposed
No. of logic components	11399	3363
No. of RAM used	According to the code rate used	2

Comparison between Base and Proposed

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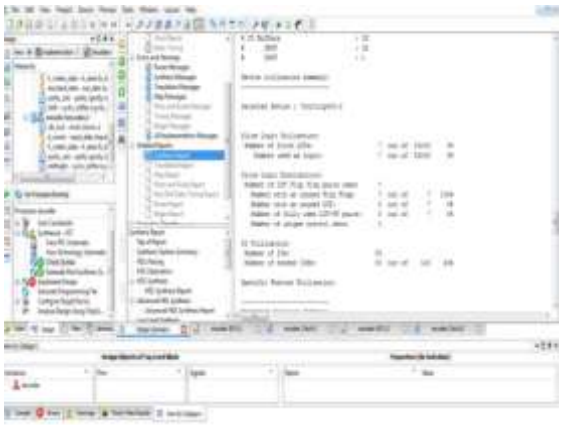
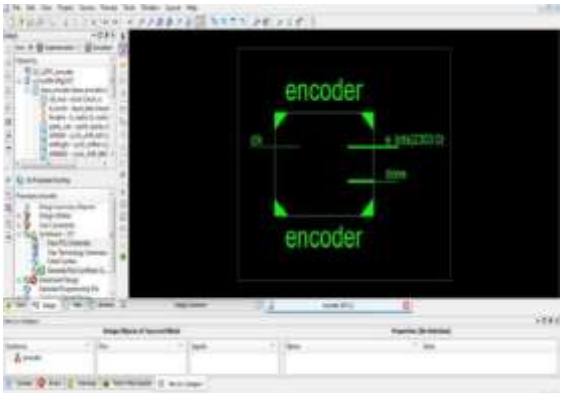
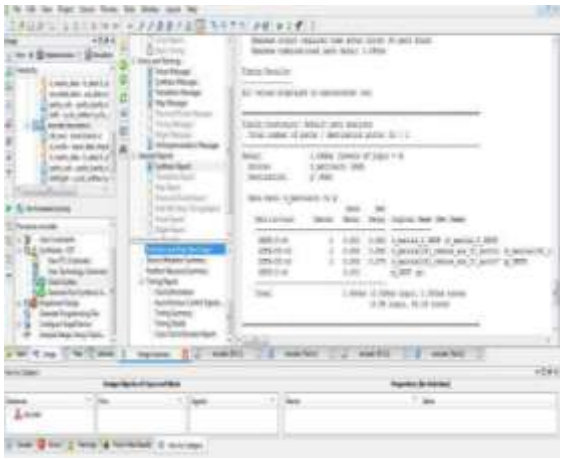


Representing the utilization of the device



RTL Schematic design of encoder



Estimated delay report

VI. CONCLUSION

In this paper, we proposed a QC LDPC encoder which utilizes a smaller number of logic components. By utilizing the dual-diagonal matrix in the proposed encoder we have decreased the complexity of the system. As the age and the calculation of the parity check matrix is going on all the while in the proposed encoder as opposed to first create the parity check matrix and afterward compute it. It saves time. Uses of cyclic shifter and rotator helps in calculation and the proposed QC LDPC encoder utilizes a smaller number of logic components. The delay time of the proposed encoder is 1.46 ns.

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