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Dynamic Field simulation for Real-Time Computers through Field Signal Simulator

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ABSTRACT:
Real-TimeComputer(RTC)Systemconsisting of Fault-Tolerant dual redundant VME bus-basedsystems (VME-1 and VME-2) with Switch over Logic Circuit (SOLC) and its associated IFMs, SCMs,PS,etc.EachVMEsystemconsistsofanED20-CPUcardanditsassociatedinput/outputcards.TheI/O status shall be indicated by LEDs. VME system receives the inputs through SCMs / IFMs fromField Signal Simulator (FSS). Outputs generated from VME systems are connected to the FSS throughSOLS. Simulation Software completely tests the systems by simulating field inputs to all the channelsof each card present in VME bins. The software also checks the healthiness of each card at every scanintervalandsendstheinformationtoDisplayStatio

The control and Instrumentation(C & I) Systemin a typical Power Planthas three layers. Thelowerlayeristhesensorsand final ControlElements,themiddlelayeristheControlEquipmentlayer &theuppermostlayersaretheDataAcquisition&SupervisionControlComputerSystems,ControlPanels,and OperatorConsoles.
The C&I subsystems of the Nuclear Power Plant(NPP) are categorized as Safety Critical, Safety-Related, and Non-SafetySystems. Safety-ThereisaSwitchOverLogic System (SOLS) which allows the outputsofVMEsystem-1orVMEsystem-2todrive FinalControlElements.

Each VMEsystem consists of an ED20-CPUcardwhichisbasedonanMC68020processor and a variety ofI/O cards for AnalogInputs (AI), Digital Inputs (DI), Analog Outputs(AO), and Relay basedDigital Outputs (ROP)cards, etc. The status of each I/O is indicated byan LED provided on the front fascia panel of thecard.

nusingTCP/IPprotocolwith10/100Mbps.

RTC systems are used for control & process systems and simulation techniques are used to achieveautomation by testing these RTC systems. It also includes RTC hardware and the software used forcontrol applications.RTC Systems are deployed to checkPlant Systems conditions and generateauthorizationoutputswhenalltheconditionsaresatisfied.

KEYWORDS:
Real-TimeComputers,DynamicSimulation,FieldSignalSimulator(FSS),Fault-TolerantSystems,C&ISystems.

I. INTRODUCTION

RelatedSystemsoftheControlEquipmentlayerconstituteamajorportionoftheSignalProcessingElectronicSystemsinaplant.
BecauseoftheSafetyassociatedwithSafety-RelatedSystems,theseSignalProcessingElectronicSystemsareconfiguredasFault-Tolerant Dual Redundant Real-Time Computers(RTC)systems.RTCsystemsareVMEbus-based systems (calledVMEsub-system-1andVMEsub-system-2).

Simulator,testingisatediousprocess.Tosimulate these heterogeneous systems we need aField Signal Simulator to feed different types ofinputs are like 0.5V to 9.5V DC, 4-20mA, PotentialFree Contact, etc., and to generate outputs formonitoringonDisplayStationandProcessComputer.

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1.2 ExistingMethodologyofTesting:

Theexistingsimulatorisusedasapassivesimulatorwith Switchesbeingprovidedforsimulating Digital Inputs, Potentiometers forAnalog Inputs, and forgeneratingDigitalOutputLEDwereprovided,and DPMsforAnalogOutputs.Usingapassivetestjig,itwas a very tedious process to test the RTC systems for all input conditions and time-consuming. A dynamic simulation technique was therefore proposed and a facility was established for this purpose. The proposed system is described below.

1.3 ProposedMethodologyofTesting:

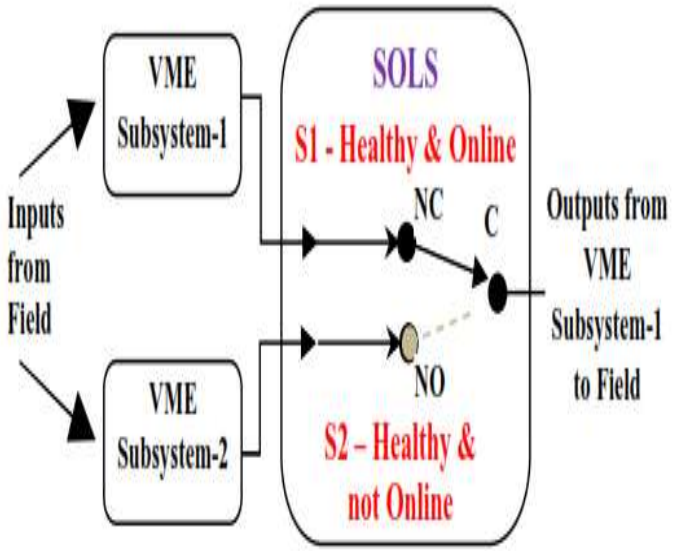

FIGURE1:SOLSSystem

TheSwitch OverLogic Systemreceivestheoutputs of VME system-1 and VME system-2 on'NO'&'NC'pinsofchangeovercontactsoflatching relays. Depending upon whether system-1 is active or system-2 is active the outputs arepassed on to the system output thru the commonPin 'C' of the latching relays. The SOLS systemhasaLogicCardthatkeepstrackofthehealthiness of VME system-1 and VME system-2and also decides which system is active. It drivesthelatchingrelaysonSOLSRelaycards.Accordingly, the contacts of latching relays areusedtoprovideoutputtothefield.

1.1 ProblemDefinition:

The Signal Processing Electronic System consistsof an ED20 CPU card and a combination of I/Ocardstomeetthesystemfunctionalityandtoanalyze theperformance.Toverifythefunctionality and performance of the system weneedtotestthesystemthoroughly.Withoutthe

This paper introduces Simulation Techniques tosimulate VME RTC Systems with Field SignalSimulator (FSS). FSS can simulate any type ofInputsignallike0.5Vto9.5VDC,4-20mA,PotentialFreeContact.InputscanfeedonSimulatortoVMEI/OcardsandgeneratereliableoutputstomonitoronDisplayStation(DS).It also implements Simulation software forautomatingtheTestingProcess.TheVMEsystem software has to scan all analog and digitalinput signals, receive the soft inputs/commandsfrom the Process computer. RTC System statussignals are to be sent to Process Computer andDisplay Station. Each VME subsystem has a dualEthernet link, which communicates with DS andFSS using TCP/IP protocol with 10/100Mbps.Figure.2showstheconnectionsbetween FSSandRTCsystems.

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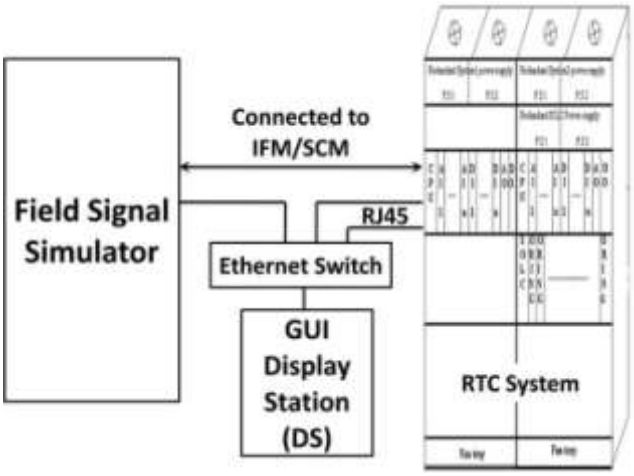

FIGURE 2:FSS forVME– RTCsystem testing

Thesystemshallsatisfythefollowingrequirements:

- Scanalltheinputsignals including softsignals
- CheckdiagnosticsofVMEsystem
- Systemoperationcycle(scantime)is1sec
- Softwareshallrunindependentlywithoutanyoperatingsystem
- Latchestheoutputs

VME system receives the inputs through SCMs,IFMs from FSS. Outputs generated from VMEsystems are connected to the FSS through SOLS.SimulationSoftwarethoroughlytestsbysimulating field inputs to all the channels of eachcardpresentinVMEbins.VMEapplicationprograms are fused fed into the EPROM of theED20-CPU card.Thesoftwarealsosendstheinformation on the healthiness of each card to theDisplayStation.

II. FAULT-TOLERANTARCHITECTURE:

RTC system is built-in fault-tolerant architecture.There is a provision to duplicate each of the inputsignals using Signal Conditioning Modules. TheSCM's also provide Field Signal isolation as wellasisolationbetween output-1tooutput-2.Theduplicatedsignalisconnectedtothetwo VMEsystems.

Both the subsystems do the processingas per the required logic and route the outputs torouting logic. When the hardware and softwarefunctionproperlythenthehealthinessofthatparticular subsystemisfedtoSOLCwhichinturndirectstheroutinglogictoroutethesubsystem'soutputs.Duringinitialpower 'ON',when both the subsystems are healthy then VME-subsystem-1outputshallberoutedtothesimulator. When VME-subsystem-1 fails,VME-subsystem-2shallberouted.WhenVME-subsystem-1becomeshealthythenalsoVME-subsystem-2 outputs shall be routed, there shallnot be any change over from one subsystem toanothersubsystemunlessthesubsystemfails.Whenboththesubsystemsfail,thefail-safeoutputshallberoutedtotheSimulator.

The healthiness of ED20-CPU and I/O boards arechecked in a 1-sec scan interval and updated theoutputsandsentthedatatotheGUIdisplaystationthroughEthernet.Whenthecardsarehealthythenthesystemshallgeneratetwopotential-freecontactoutputsassystemshealthinessthat gotoSOLC.

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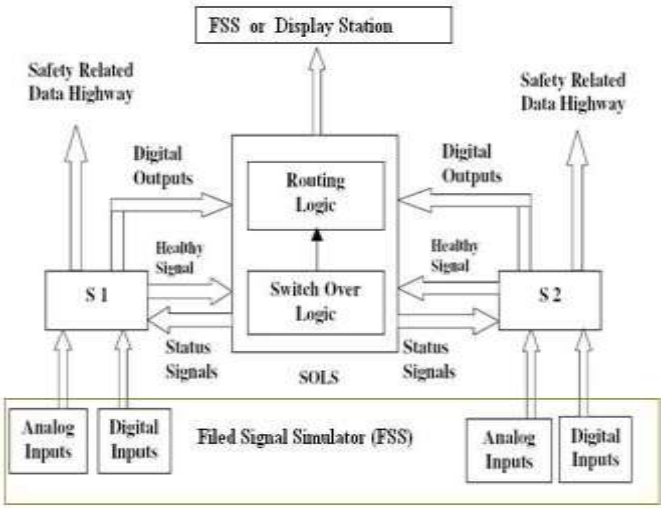

FIGURE3: Fault-TolerantArchitecture

III. VME SYSTEM CONFIGURATION

VME (Versa Modular Euro) systems are locatedinthisElectronicCabinet.TheycanhandleSafety-Critical as well as Safety Related signals.In the case of Safety-Critical, it is triplicated &SafetyRelatedisduplicated.Hencedualredundant VME systems with SOLS are used forprocessingthesesignals.Toconnectthefieldinput signals to both the VME systems, all digitalinput signals are multiplied using relays with two change-overcontactsprovidedonIFMs.ForconnectingAnalog signalstoboththeVMEsystems 1:2 Analog signals conditioning modulesare used. Then SCMs have one input and twoisolatedoutputs.OutputsfromboththeVMEsystems are connected to OR-ing logic cards ofSOLS, which routes the healthy system's outputstothefield.

TheCabinetconsistsofVME-subsystem-1anditsredundantsystemVME-subsystem-2alongwith their associated power supply units. SOLSsystemisalsolocatedalongwithitspowersupply unit. The ED20 and combination of I/Oboards are not hot-pluggable. In case of failure ofany board, power is to be switched off for therespective system, the board is to be replaced andthen power is to be restored for that system. RTCsystem can house any combination of I/O boardsbasedonthesystemrequirements.

Components oftheVMESystems are like:

- **VMEBus**
  - **P1-Backplane(VME-Motherboard)**
  - **P2-Backplane(I/O-Motherboard)**
- **ED20-CPUCard**
- **AnalogInputCard**
- **DigitalInputCard**
- **DigitalOutputCard**
- **AnalogOutputCard**
- **Synchro-DigitalConversionCard**
- **OpticalEncoderInputCardetc…**

ComponentsofSOLSSystemare like:

- **SwitchOverLogicCard**
- **ORing LogicCard**
- **P1-Backplane**
- **P2-Backplane**

ThefollowingstepsaretobecarriedoutforVMEsystem configuration.

i. PlacetheproperprogrammedEPROMsin the respective places of the ED20-CPUcard.

ii. SystemIntegrationTestProcedureprovides the details about the number ofI/O cards required for a particular system.The maximum number of channels thateach cardcansupportisgiveninTable-1.

iii. SettheI/Ocardaddressesintherespective I/Ocard throughjumperselection.

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I/O Card	No. ofChannels percard
AnalogInput	30
DigitalInput	30
RelayOutput	15
AnalogOutput	4
SDCcard	3
Opticalencodercard	3

TABLE1:I/OCardsCapacity

In a single VME system, only one CPU card and nineteen I/O cards can be populated. Similarly, in the SOLS system, only one SOLC and nine OLC cardscanbepopulatedaccordingly.

IV. FIELD SIGNAL SIMULATOR

TheComputer-basedControlSystemacquiresvarioustypesofphysicalparameters,suchastemperature, pressure, flow, strain, position, andspeedusingelectronicequipment/modules/boards.

The collected data is sent to a computerfor analysisanddisplay.The control systemsalsotakeaction(control)basedonthedatareceived.TurningON/OFFlamps,motors,valves,heaters,andfansarecommonfunctionsof control.Sending out voltage, current, digitalwords, pulses, and waveforms are also functionsoftheControlsystems.Embeddedsoftwarerunning in the computer coordinates and executesthesefunctions.

ECIL is equipped with state of art Field SignalSimulator(FSS)toperformthefunctionalandacceptancetestsbeforesendingthesetypesofequipmenttovarioussites.

FIELD SIGNAL SIMULATOR is designed tosimulate thefieldparameters are like:

1. Thermocouples(K–type)Output
2. AnalogOutput(0-10V,0-10mV,0-24Vor 4-20mA)
3. AnalogInput(4-20mA)
4. DigitalOutput
5. RelayInput
6. OpenCollectorInput
7. LeakDetectionOutput
8. RTDOutput
9. SynchroOutput
10. EncoderOutput

4.1 SystemArchitecture

The FSSis housed in standard racks with 19”card frames. The systemoperates on a single-phase230V,50Hz, ACpowersupply.Theinstrumentation is PXI and VME based, with anIndustrialcomputerforsimulationoffieldsignals.A high-speed Ethernet link connects theIndustrial computer and the CPU module on thePXI bus. The system is designed to work up to55 degrees Celsius.Battery back-up is providedfor conducting the burn-in tests. Video graphicdisplay, keyboard, mouse, and color printer areconnectedtothePXIbus-basedINTELCPUboard.

4.2 DataAcquisition andControl:

The MS Window operating system runs on theIntelPentiumCPU,onwhichtheapplicationsoftwareisdevelopedusingNationalInstrument’sLABVIEW. Theapplicationsoftware generates the field data for the signalconditioning boards using the hardware modules.The response parameters of the unit under test areread by the CPU.The FSS generates the testreports based on the Accepted Test Procedure oftheUnitUnderTest(UUT).

4.3 I/OConnections:

FSSinputsandoutputsareterminatedonterminalblocksinternally.Allthecablesarecolor-coded andlabeledforeasyidentification.A separate rack is provided for storing the cablebunches, whenever the system is not in use.Allinputs and outputs are available simultaneously;nomultiplexingofthesignalsisdone.

ThemaximumnumberofsignalsthatFSSsupportsisgiveninTable-2.

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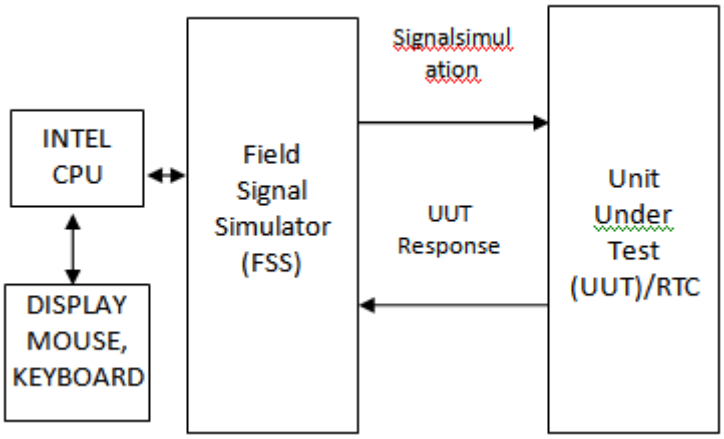

FIGURE 4: Blockdiagramoftheunitundertestwith Field signalsimulator

4.4 FSS Software:

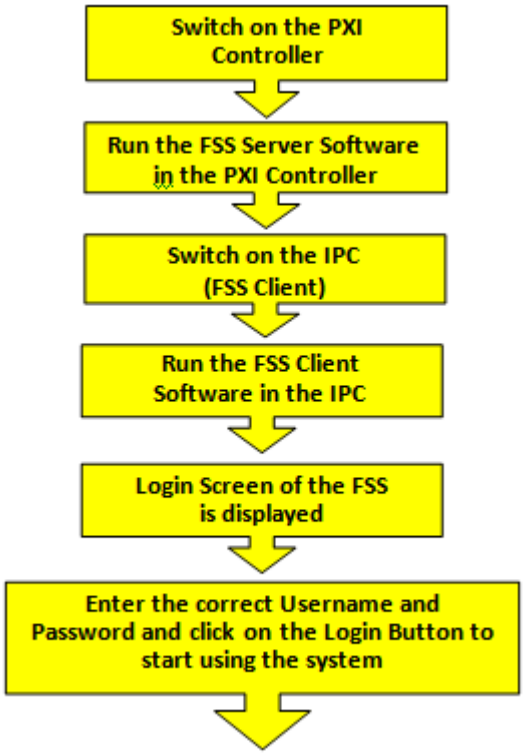

FIGURE5: SwitchonProcedure forFSS Server&Client

FSSsoftwareisgenericsoftwaretosimulateth at field signals for a Computer-based controlandinstrumentationsystem.FSSsoftwarework sinconjunctionwithPXI,VME,andCRIObasedhardw aretosimulatethefieldsignalsfortheComputersbasedc ontrolandinstrumentationpanel.Itsgeneral-purposenatureeasilyextendsitscapabilitiestobuildan dperformsspecificUUTtestroutines.

The FSS software is built following a "Client-Server" model. The FSS system consists of a PXIcontroller and twoIPCs. PXI controller servesprimarily as the Server and IPCs as Clients. OneoftheIPCwillbedesignated as the "Development Station". Either the PXI-controllerortheIPCscanbeusedas"DevelopmentStati

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on". It is recommended that PXI-Controllershouldnotbeusedasadevelopmentstationw hile it's running the server software. Likewise,IPCssoftwareshouldnotbeusedasadevelop ment station when it's running the clientsoftware.

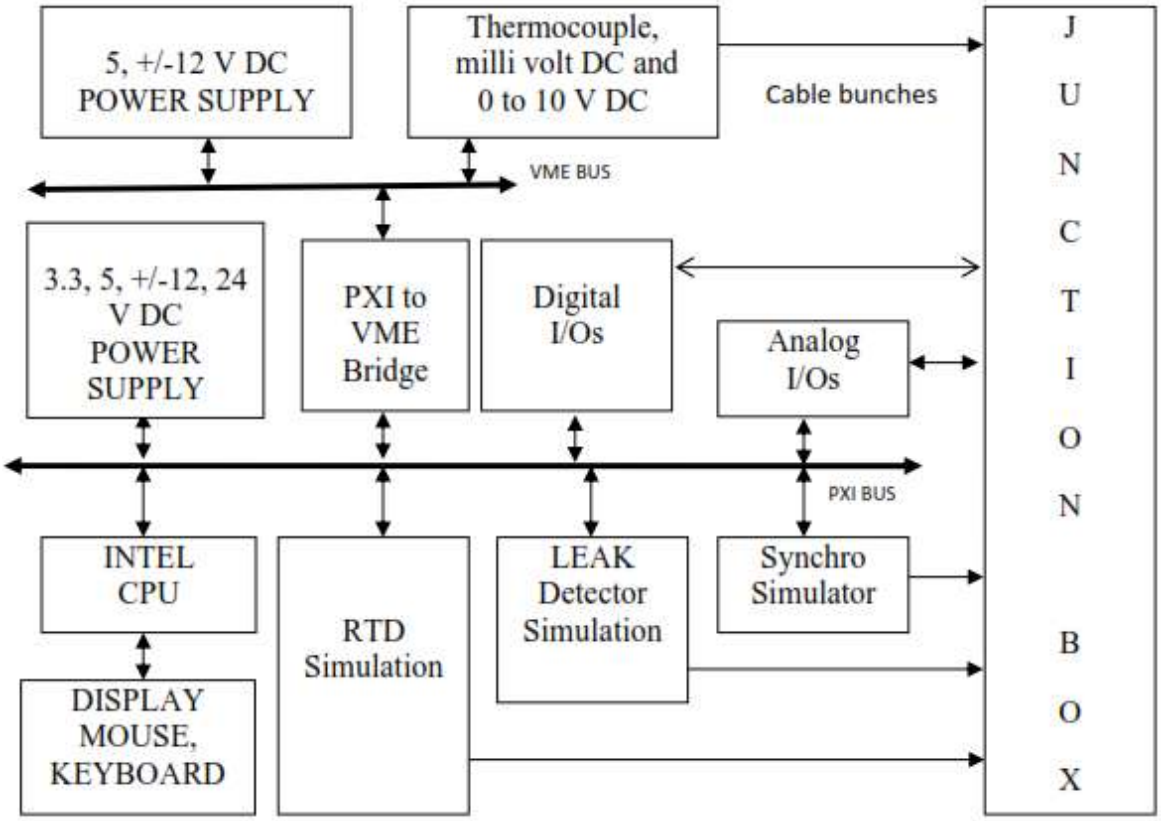

FIGURE6: BlockdiagramFieldsignalsimulator

The server software in the PXI-controller runs inthe background when it is launched. It should belaunched before any client software is launched.ThePXI-Controller canalsoactasa clientinaddition to being the server. Thus, we can run theclient software on the PXI-controller itself whichputs the usage of two IPCs as additional clients,onlyonaneedbasis.

ThefollowingarethemajormodulesoftheClientsoftw are:

i) **CreateUUTinfo:**CreateUUTinfoutilityallows the user to create a file that stores theinformation about a Unit under Test like tags,FSSLogicalchannelsused,IPAddresses,Ch annelMapping,etc. ThisutilityreadstheUUT Tag configurationfromthe UUT terminalinfo file. This is an excel file with a definedformat. The user will have to enter the Tagsand their terminal information in this file. Thisutility also reads the UUT Soft Input Info file.This is also an excel file where a user entersthedetailsofthesoft input.

ii) **I/O Explorer:** I/O Explorer allows the user toconfigure, read and write values for each typeofchannel.Userscandirectlyupdatevalueson different channels interfaced with the VMERTC system under the testing and observe theUUTbehaviorandresponsetotheFieldSimulat edSignal fromFSSSystem.

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FIGURE7:I/OEXPLORER–HomeScreen

I/O Explorer also helps the user of the system toestablishtheintegrityinsignalconnectivitybetween the FSS system and the UUT. Throughthe I/O Explorer user can set a value on a channelandmeasurethevalueusinganexternalmeasuri ngdevicebeforeconnectingittotheappropriate channel or the terminal of the UUT.This ensures that the right channel of the FSSsystemisconnectedtotheUUT.

ThefollowingarethemajormodulesoftheServersoftw are:

i) **DAQCore:**Thismodule istheheartof theFSSsoftware.DAQCoreimplementshardware-levelinteractionwiththePXI,VME,and CRIOwhichconstitutestheFSSsystems. Itcalls the APIs built for the FSSsystems and executes the commands sent bytheClients.DAQCoreisasinglemodulethrough which all interaction with all differenttypes of hardware used in the FSS system ispossible.DAQCoreimplementsacommonI/O read/write errors handling mechanism andit also returns the value that is set through thecommands.

FIGURE8: Server–SystemStatus

ii) **CommandRouter:**Theserverhoststhecomman droutermodule.CommandRoutermodule is used for identification of the origin ofcommandfortheDAQCoretoexecute.Afterthe command is executed by the DAQCore theresponse is again routed through the

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CommandRoutertothesource.Thecommandrout ermodule also sorts the commands from varioussources and segregates them based on the signaltype for the DAQCore to execute. The source ofthecommandcouldbeanywhere.

4.5 FSS Server:

The first FSS server software is launched on thePXI-controller.Theservershouldbelaunchedbefore launching the client software of the IPCsor on the PXI-Controller. The client displays anerror message if the sequence is not followed.FSS Software runs on the background with itsicon minimized to the windows taskbar icon tray.The Server application also displays the healthparametersoftheFSSsystemsaswellastheclient sthatareconnected.
The Server module interacts with the hardware ofthefieldsignalsimulationsystem.Theservermodule is responsible for reading and writing toallhardwareI/Os.

Server Software: The Server Software is mainlydividedintothefollowingmodule:

1. **DAQCore:** Service hardware commandsfrommultiplemodulesofthemainsoft ware.
2. **DAQ Engine:** Provides abstraction fromhardwaretoothermodulesof the mainsoftware.
3. **Settings:** Provides settings to the user toconnectusingMXIorTCP/IP.
4. **Calibration:** Provides channel calibrationtotheuser

4.6 FSSClient:

After the launch of the FSS server on the PXI-controller, FSS client software is launched eitheronthePXI-controllerorontheIPCs.

Clientsoftwarehasanaccessprivilegesetup.First,theu serhastolog intotheclientsoftwarewiththeappropriateloginIDand password.AccordingtotheprivilegessetforlogicID,fe aturesoftheclientsoftware willbeavailableorunavailabletotheuser.
Basedonthesuccessfulloginttheclientapplicationenter sthehomescreen.

Userscaninitiatethesystemconfigurationasfollows.

1. CreatetheUUTInformationfile
2. FSStoUUTconnectivityfile(LogicChannelMap ping)
3. LaunchI/OExplorer
4. TestFSSandUUTconnectivity
5. GenerateTestReport

ClientSoftware: TheServerSoftwareismainlydivide dintothefollowingmodule:

1. CreateUUTInfo
2. I/OExplore

V. TESTING

For System Integration Test, two different typesof software are to be developed. One is system softwarethat runs on VME based RTC systems and the second software is GUIwhichrunsonPC/DisplayStation.ThisGUIsoftw areisuser-friendly,easily configurable, enabling the tester to use thesame software for different I/O configurations ofthe VME-RTC system without much change inthesoftware.

Two sets of programmed EPROMs named (S1Odd, S1 Even & S2 Odd, S2 Even) are providedtotesttheVME-RTCsystemswithdualredundantarchitecture.One set of EPROMs aretobeusedforVMEsubsystem-1(S1)andanother set of EPROMs are to be used for VME subsystem-2 (S2). GUI software is to be installedonthePC.

In GUI software, provision is available to selectthenumberofI/Ocards(AI,DI,RO&AO,etc.)asp ersystemrequirements,andthesameis communicated to the VME ED20 CPU cardthrough TCP/IP protocol. Based on the selection,VME Application software scans the inputs andlatchestheoutputs.

TwoEthernetportsareavailable in each system and the scanneddata aresenttobothportssimultaneously.Thedatareceived from both ports can be viewed in theGUIsoftware.

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FIGURE9:VMERTC-I/OSimulationGUIinLabVIEW

FIGURE10:VMERTCsystemwithI/Osimulationthru FSS

TheIntegrationandSystemTestingprocessfocusesonthefunctionalexternals,testingtouncovererrorsandtoensurethatthedefined input will produce actual results that agree withrequiredresults.

SystemIntegrationandtestingprocesscanbe carried out as per Detailed Test cases mentionedin the Test Procedure.Test Procedure should bedefined for each hardware and software to checkthe functional and performance requirements tobe met. It should also be defined (hardware &softwareintegrationandtestprocedure)forassembled hardware and integrated software ofeach sub-system to check the integrity of bothhardware and software. Test Reportsshould begeneratedaccordingly.TheTestresultsandobservations shall be recorded in a document forreview/auditduringVerification andValidation (V&V).

Requirement for the design of online diagnosticsfor VME hardware/software should be specifiedto detect various faults in the hardware/software,data, or code corruption and to take appropriateactions.Thisshouldincludeidentification

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ofsystem resources to be checked, diagnostics onsystem start-up, and during run-time on detectionoffaults.Inaddition,the designmustprovidebuilt-in features for online fault detection, faultindication,anddrivingfail-safeoutputs.

AllthecardsdesignedontheVMEbusincorporate extensive online diagnostics featuresfor fault detection and health monitoring throughthe watchdog timer. The watchdog timer formstheheartbeatoftheentirecomputersystem.Since plantoutputsarecontrolledthroughtheactuation of relays, watchdog features were alsointegratedintotheMono-shotRelayOutputboard. This ensures that, in case of either systempower failures or the failures of the ED20 CPUsoftware, the plant outputs terminate to fail-safemode,thuspreventingthecatastropheontheoperatingplant.

Sl.No	SignalType	SignalRange	Signal Characteristics	Number of Channels
1	Analog Outputs(SignalGeneration)	K-TypeThermocouple	0.5°Cresolution	500
		0-10mVDC	14-bits @25 mV FSR(equivalentto1.53µVStep)	16
		0-10VDC	14-bitresolution	600
		0-24VDC	14-bitresolution	20
		4-20mA	14-bitresolution	75
2	DigitalOutputs (SignalExcitation)	Drycontact	24VDC,electro-mechanical	650
3	AnalogInputmonitoring	4-20mA	14-bitresolution	10
4	RelayInput Monitoring	Drycontact	24VDC,electro-mechanical	350
5	Open-collectormonitoring	Open-collector	(VCE)SAT≤1.5V	50
6	RTD(Pt-100)sensorsimulation	-200°Cto850°C	ΔI°C (equivalentto 0.3ΩStep)	30
7	LeakDetector(LKD)signalsimulation	Resistance armSimulation	0Ω,470Ω,570Ω,Open	350
8	Encoder	Angles in degrees	0 ° to 360 °	25

TABLE2:Maximum number ofSignalssupportsFSSsystem

VI. VERIFICATION&VALIDATION (V&V)

Thecomputer-basedcontrolsystemshavetomeet not only the functional performance but inadditiontheyhavetomeettheregulatoryrequirements likeenhancedreliabilityandavailability.Redundancy andfaulttolerancefeatures are to be provided and the overall systemdesign should have a high mean time betweenfailures and low mean time to repair to achievebetterreliability.

Thebelow Figure-11showsthe designofreal-time computers of both hardware and softwaresub-systems which are subjected to the system Verificationand Validationprocess.Atthebeginningofthesystemdevelopment,verificationplansandproceduresshallbeproducedwhichshallcoverhardwareverification,software verification,and system validation.

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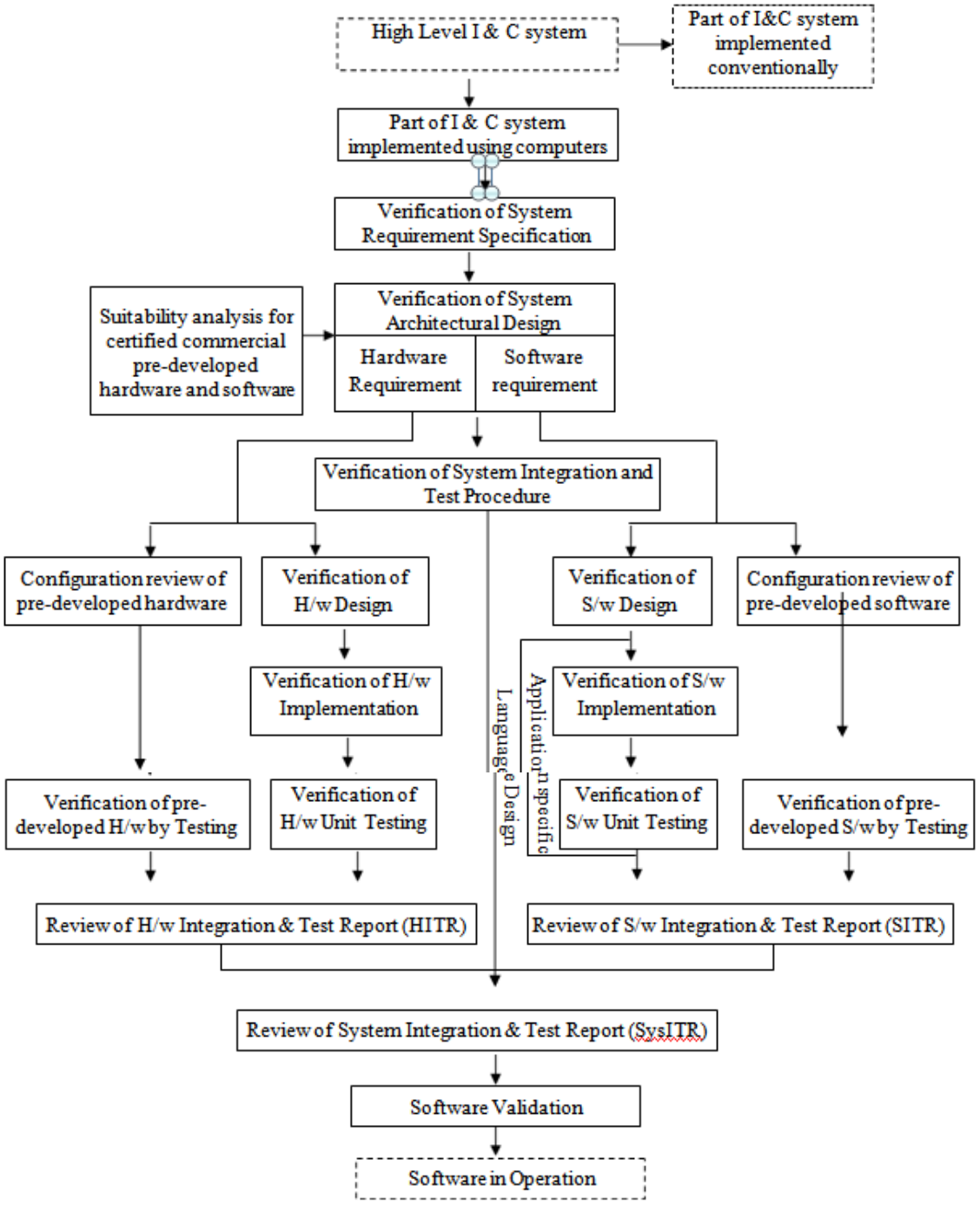

FIGURE11: SystemVerification&ValidationProcess

VII. CONCLUSION

Morethan100RealTimeComputerbasedcontrolsystemsforPowerPlantControl&Processapplicationshavebeendevelopedandtestedwith FieldSignalSimulator.Dynamictesting has ensured timing cycles and speeded upthetestingtimedrastically.Thismethodoftesting can be adopted for any Microprocessor,Microcontroller,andcomputer-basedsystem.

VIII. FUTUREENHANCEMENT

The process of inter-connectingthe FSS tothesystemundertestis tedious and cumbersomesinceitinvolvestheconnectionofdiscrete

wires.Thistypeofwiringgivesalotofcontactproblems. Tracingtheproblem and rectifyingisatime-consumingprocess.

Toreducetheinter-connectiontime,itisproposed to make suitable arrangements at FSSandthesystemundertestsothatFlatcablescanbeusedtoquicklyinterconnectthesystems.Thisrequiresmodification ofinterface terminal blocks at the micro-computersystem under test by providing one more IDCheaderonIFM.AttheFSSendscrewedterminalsaretobeinterconnectedtoanadditionalIFMwithanIDCconnector.Thus,theIDCconnectorismadeavailableatbothendsacrosswhichaFlatcablecanbeconnected.This willensure a drasticreductioninoveralltestingtimeandbettertimeutilizationoftheFSS.

Currently,thetestprogramsarewrittensothatthesystemgivestheoutputdetailsforthespecifiedinputs.Thequalitycontrolengineersareexpectedtocomparethetestresultswiththeexpectedvaluesanddecidewhetherthesystemhaspassedorfailed.

Inthenextphaseofimprovement,itisproposed to modify the test programs such thatthe FSS by itself compares the test results withthe expected values and declares to the qualitycontrolengineerswhetherthesystemshavepassedorfailed.Thiswillensureareductionintestingtimeandhumanerrors.

Currently,alimitedtypeofsignalsnamelyCurrent,Voltage,Thermocouple,RTD,LKD,Synchro, and Encodertypeofinputscanbetested.Itisproposedtoenhancethiscapabilityforothertypesofinputslikeflow,pressure,etc.

Complex C & I system with a large number ofI/Os.TheI/Ocapacityofeachsignalisexpectedtobeenhancedbytheadditionofboards of various types. This will be useful fortesting.

BIOGRAPHIES

Shri.A.K.Asthanawas born in Hyderabad,AndhraPradesh,onJune09,1955.HegraduatedinElectronics and Communication Engineering fromJawaharlalNehruTechnological University, Hyderabad,India.Hejoined asaGraduateEngineerTraineeinElectronics CorporationofIndiaLimited,Hyderabadin the year 1979.Sincethen,hehad beenworkingon C & I systems for Pressurized Heavy WaterandFastBreederReactors.Heworked asGeneralManagerand retiredin the year 2015,Control andSystemsGroupofElectronicsCorporationofIndia Limited,Hyderabad.Hepublishedapaper entitled"PFBRand PHWR Reactors–C& I Perspective" in ISA – POWID – INDIA in2010.

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REFERENCES

[1] AERBSafetyGuideforComputer-basedsystems–AERB/SG/D25
[2] PROJECTHandBook
[3] UserManualforFieldSignalSimulator
[4] Real-TimeComputer-BasedControlSystemsfor PrototypeFastBreederReactor
[5] IEEERecommendedPracticeforSoftwareDesignDescriptions–IEEEStd1016-1998
[6] IEEE Recommended Practice for SoftwareRequirementsSpecifications–IEEEStd830–1998.