International Journal of Advances in Engineering and Management (IJAEM)
Volume 5, Issue 7 July 2023, pp: 76-85 www.ijaem.net ISSN: 2395-5252

Automatic Bottle Filling Plant Controller using VHDL

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Date of Submission: 25-06-2023 Date of Acceptance: 07-07-2023

ABSTRACT
In this paper, we present a research project ondesigninganautomaticbottlefillingplantcontroller using VHDL code. The controller isdesignedtoautomatetheprocessoffillingbottleswith a specified quantity of liquid. The projectaimstoincreaseefficiency,reducewaste,andeliminate errors in the filling process.VHDLcode is used to program a field programmablegatearray(FPGA).Thesystemistested andsimulatedusingVIVADOsoftware,andtheresults show that the system is able to fill bottlesaccurately andefficiently.

Keywords: Automatic Bottle Filling Plant,VHDL Code, Basys3 (FPGA Board) , VivadoSoftware.

I. INTRODUCTION:

The efficient filling of bottles is a crucial task invariousindustries,includingbeverage,pharmaceutical,andchemical.Toautomatetheprocessandensureaccuracy,automaticbottlefillingcontrollers have been developed. In this researchpaper,weaimtodesignandimplementanautomaticbottle filling controller using VHDL, a hardwaredescriptionlanguagecommonlyusedindigitalcircuitdesign.OurprojectinvolvestheuseofVHDL to create a digital circuit that controls thefilling of bottles based on input parameters such asvolume and speed. The goal of this project is toprovideareliable,accurate,andcost-effectivesolution fortheautomaticfilling ofbottles.

Theprimaryobjectiveofthis project istodesignandimplement areliable,accurate,andcost-effectivesolutionfortheautomaticfilling ofbottles.Indoingso, wehopetoprovideasolutionthatcanbeeasilyimplementedinvariousindustries andcanimprovetheefficiencyandaccuracy ofthefilling process. TheuseofFPGAwillenableustocreateadigital circuitthat isflexible,scalable,andcanbeeasilymodifiedtomeetthespecificrequirements ofdifferentapplications.

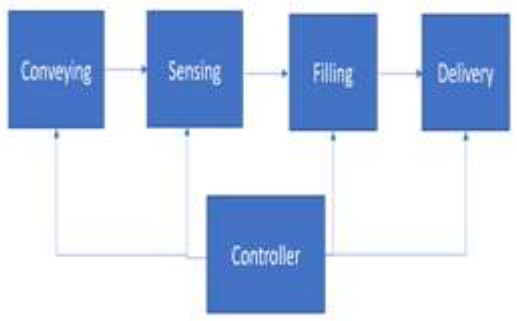

Fig1.1BlockDiagramofautomaticbottlefillingcontroller.

Fig.1.1 shows the block diagram of states in automatic bottle filling plant controller. There are four states in this diagram i.e conveying, sensing, filling and delivering. All that's process are controlled by the controller as shown in fig.1.1.

2. Operations:

The operation of an Automatic Bottle Filling PlantControllertypicallyinvolvesthefollowingsteps:

1. BottleDetection:Thesystemdetectsthepresenceof a bottle using a sensor. If a bottle is present, thesystemproceeds tothenextstep.
2 Liquid Level Detection: The system detects thecurrent level of liquid in the bottle using a sensor. Iftheliquidlevelisbelowthedesiredlevel,thesystemproceeds to thenextstep.
2. Valve Opening: The system opens the valve toallowthe liquid to flowinto thebottle.

3. Liquid Filling: The liquid flows into the bottleuntiltheliquidlevelreachesthedesiredlevel. During this process, the system monitors the liquidlevelto preventoverfilling.
4. Valve Closing: Once the desired liquid level isreached,thesystemclosesthevalvetostoptheflo wofliquid.
5. Bottle Removal: The system detects the removalof the filled bottle and waits for the next bottle to bedetected.

Throughout the operation, the system continuouslymonitors the filling process to detect any errors orabnormalities. If an error is detected, the systemstopstheoperationandalertstheoperator.Thesafety features of the system prevent overfilling oranyotherhazards.Theentireoperationiscontrolledby the microcontroller, which is programmed usingVHDL code. The VHDL code defines the behaviorof the system and its interactions with the sensors,actuators,andothercomponents.

II. FINITE STATE MACHINE (FSM):

Afinitestatemachine(sometimescalledafinitestateautomaton)isa computationmodelthatcanbeimplementedwithhardwareorsoftwareandcanbeusedtosimulatesequentiallogicandsomecomputerprograms.Finitestateautomatagenerateregularlanguages.Finitestatemachinescanbeusedtomodel problemsinmanyfieldsincludingmathematics,artificialintelligence,games,andlinguistics.
ThearetwotypesofStatemachines:
1. MealyMachine
2. MooreMachine

2.1 Mealy Machine:

Inmealymachineoutputdependsbothuponthepresent state and the present input.The value of theoutputfunctionisafunctionofthetransitionsandthe changes, when the input logic on the presentstateisdone.Mealyoutputsareasynchronous.Theycanchangeimmediatelywithinputchange,independentoftheclock as shown in fig 2.1.

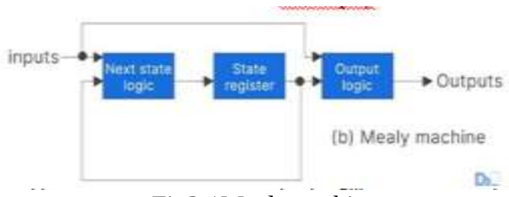

Fig2.1Mealymachine.

2.2 Moore Machine:

In Moore machine output depends only on thepresentstate.Thevalueoftheoutputfunctionisafunctionofthe current state and the changes at the clockedges,wheneverstatechanges occur.as shown in fig 2.2.

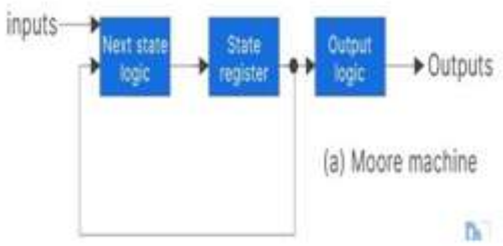

Fig2.2Mooremachine.

III. RELATED WORK:

1. AutomaticbottlefillingsystemsusingPLC:Programmablelogiccontrollers(PLCs)havebeenwidelyusedforautomationinvariousindustries, including bottle filling. PLC-basedautomaticbottlefillingsystemshavebeendeveloped and implemented, which use sensorsandactuatorstocontrolthefillingprocess. These systems have been found to be reliable,accurate,and efficient.
2. Automaticbottlefillingsystemsusingmicrocontrollers:MicrocontrollerssuchasArduinohave alsobeenused forautomatingbottlefilling. Thesesystems usesensors andactuators,andthemicrocontrollerisprogrammed to control the filling process basedon the input parameters. These systems havebeenfoundtobecost-effectiveandeasytoimplement.AutomaticbottlefillingsystemsusingLabVIEW:LabVIEWisagraphicalprogramminglanguageusedforautomationanddataacquisition.Ithasbeenusedtodevelop automaticbottlefillingsystems,whereLabVIEW is used to control the filling processand monitor the system. These systems offer auser-friendly interface and real-time monitoringcapabilities.
3. Research on sensors for bottle filling: Sensorsplay a crucial role in the automatic bottle fillingprocess, as they are used to measure the volumeofliquidandregulatetheflow.Therehavebeenvariousstudiesonthedevelopmentandevaluationofsensorsforbottlefilling,includingultrasonic,capacitive,andopticalsensors.Thesearesomeexamplesofrelatedworkinthe
4. areaofautomaticbottlefillingcontroller

Parameters	Programmable Logic controller	Field Programmable Gate Array
Purpose	Industrial control and automation	General-purpose programmable device.
Functionality	Sequential and logic-based control tasks	Custom digital logic and algorithms.
Programming	industrial-specific languages.	Hardware description languages like VHDL or Verilog.
Power Efficiency	Power loss is more than FPGA	Power optimization based on application requirements.

IV. IMPLEMENTATION:

In our research paper a state machine diagram isdesigned for the desired state machine which cancontrolthewholebottlefillingprocessautomatically. The system requirements include theinputsignalsfromtheliquidlevelsensors,theoutput signals to control the valves and pumps, andthe processing blocks required to calculate the flowrate of the liquid. the system is able to detect whenthe bottle is full and stop the filling process. TheVHDL architecture for the system will consist ofinput, output, and processing modules. The inputmodule will be responsible for receiving the signalsfromthesensors,theprocessingmodulewillcalculate the flow rate and control the valves, andtheoutputmodulewillcontrolthesignalstostopthefilling process when the bottle is full. And so on forremainingstateslikecapping,labelling,qualitycheckingand packaging.

The VHDL code will be written for each module,includingtheinput,processing,andoutputmodules.The VHDL code will be verified using simulationsoftware to ensure that it is functioning correctly.The simulation software will provide a waveformthatshowstheinputandoutputsignalsofthedigitalcircuit.Byanalysingthewaveform,thedesignercanverifythattheVHDLcodeisperformingtherequired calculationsandproducingthecorrectoutput signals.After verifying the VHDL code, thenext stepistosynthesizetheVHDLcode.Thisinvolves translating the VHDL code into a gate-level netlist, which describes the logic gates andtheirinterconnectionsrequiredtoimplementthedigitalcircuiton theFPGA.

Once the VHDL code is synthesized, the next stepistoplaceandroutethedesign.Thisinvolvesmapping the logic gates onto the FPGA and routingthe connections between them.Finally, the FPGAcanbeprogrammedwiththesynthesizeddesignandthe system can be tested to ensure that it meets thesystem requirements. If any issues are found, theVHDL code can be modified and the synthesis andplaceandroutestepscanberepeateduntilthedesignis functioning correctly.

Name	Direction	Description
clk	INPUT	Usedto giveclocksignal.
reset	INPUT	UsedtoResetthesystem

empty_sensor	INPUT	Usedtocheckwhetheremptybottl e isdetectedornot
full_sensor	INPUT	Usedtocheckwhetherbottleis filled ornot
cap_sensor	INPUT	Usedtocheckwhetherbottleisper fectlycappedornot
quality_check	INPUT	Usedtocheckqualityoffilled&La belledbottle
packeging_done	INPUT	Usedtogive informationaboutpackaging
valve	OUTPUT	Valve to fill thebottles.
conveyor	OUTPUT	Conveyor
capper	OUTPUT	Usedforcapping.
labeler	OUTPUT	Usedtolabelthebottles.
checking	OUTPUT	Usedforqualitychecking

Table1.Input/Outputswithremarks.

4.1 Field Programming Gate Array(FPGA)

A field-programmable gate array (FPGA) is asemiconductordevicethatcanbeconfiguredbythe designer after manufacture, hence the name"field-programmable".FPGAsareprogrammedusingalogiccircuitdiagramorhardwaredescription language (HDL) source code. Thisprogram is reprogrammable by the designer ifnecessary.IftheFPGAisprogrammedbythe user, the user can also modify or change theprogram.TheimplementedprogramintheFPGA shows the operation of the chip or kit.Theycanbeusedtoimplementanylogicfunction that an application-specific integratedcircuit (ASIC) might perform, but the ability toupdatefunctionalityafterdeliveryoffersadvantagesformanyapplications.FieldProgrammableGateArrays (FPGAs)arewidelyused in rapid prototyping and proof of conceptdesign as well as in electronic systems wherecustomICmaskmanufacturingisreallyexpensive due to small quantities. The systemwasimplementedinhardwareusingFPGABasys 3. According to the design procedure, itstartswiththedescriptionofthecircuit,inwhich the whole circuit is designed by logic,whichisdoneusing(VHDL).Afunctionaldescription was then performed, followed bysynthesis and post-synthesis simulations. Thenthe implementation and time simulation takesplace and the generated file is downloaded tothe target device. This system used as a targetdeviceisanFPGAkit.Circuitdesignordescription can be done using VHDL followedbyfunctionalsimulationandsynthesis.Thedesign flow is followed until timing simulationandthenthegeneratedfileisdownloadedtothetargetdevice(FPGA).FPGAshavegainedrapidadoptionand growthover thepastdecadebecausethey canbeusedinaverywidevarietyof applications. A list of typical applicationsincludes: random logic, integration of multipleSPLDs,devices

4.2 Basys3 Board:

The Basys 3 is a versatile developmentboardthatprovidesahands-onlearningexperiencefordigitaldesignandFPGAprogramming. It offers a range of features andcapabilitiestosupportprojectdevelopmentandexperimentation.Theboard'sXilinxArtix-7FPGAisapowerfulprogrammablelogicdevicethat allows users to implement custom digitalcircuits.With33,280logiccells,1,800KbitsofblockRAM,and90DSPslices,theFPGAprovidesampleresourcesforcomplexdesigns.

TheBasys3boardincludesvariousinput/output interfaces that enable interactionwiththeboardandexternaldevices.Theseinterfaces include user switches, LEDs, pushbuttons,seven-segmentdisplays,VGAoutput,USB-UARTbridge,andPmodconnectors.Thesefeaturesallowforuserinput,outputdisplay, and connection with peripherals. Fordata storage, the board provides 256 MB ofDDR3memory,whichcanbeusedtostoredataduring operation.Additionally,ithas16MBofQuad-SPI flash memory that allows for non-volatilestorageofFPGAconfigurations,ensuringeasy reconfigurationof theFPGA.

Insummary,theBasys3boardisapopular choice for digital design and FPGA-based projects. Its Xilinx Artix-7 FPGA, I/Ointerfaces,memorycapabilities,educationalresources,andexpandability makeitavaluabletoolforlearningandprototypingdigitalcircuitsandembeddedsystems.

Fig4.2 Basys3kit

TheBasys3isasmallcircuitboardthathelps people learn about digital logic designusing a technology called Field-ProgrammableGateArrays. It has a special chip called the Xilinx Artix-7 FPGA that can be programmed to perform different tasks. The board has buttons, switches, lights, and displays that you can use to interact with your circuit designs and see the results. It also has USB ports, a UART port, and an Ethernet port to connect to other devices like computers.To make the Basys 3 work, you use software called Vivado Design Suite or similar tools. These tools let you write and test your circuit designs, and then program the FPGA on the board. The Basys 3 is commonly used in schools and by hobbyists to learn about digital circuits and how to program FPGAs.

V. DESIGN METHODOLOGY:

The system consists of a filling machine, aconveyorbelt,sensors,andanFPGA-basedcontroller. The filling machine is used to fill thebottleswiththeliquid,andtheconveyorbeltisusedto transport the bottles to the filling machine. Thesensors are used to detect the presence of bottles ontheconveyorbeltandthelevelofliquidinthefillingmachine. The FPGA-based controller is responsiblefor controlling the filling machine, conveyor belt,and sensors.

TheVHDL codeisusedtoprogram theFPGA with the necessary control signals. The codeisdesignedtomonitorthesensors,controltheconveyor belt, and fill the bottles with the requiredamountofliquid.Thecodealsoincludeserrorhandling routines to detect and correct errors in thefilling process. Theprovided code represents thebehavioral description of a bottle filling controllerusingaFSMapproach.Itdefinesanentitycalled`bottlefillingplantcontroller`withinputandoutputportsforvarious signals and control lines.Thearchitectureblockdescribes the behavior of the controller. Ituses a clock (`clk`) and a synchronous reset signal(`reset`) to control the state transitions and actionswithin theFSM.

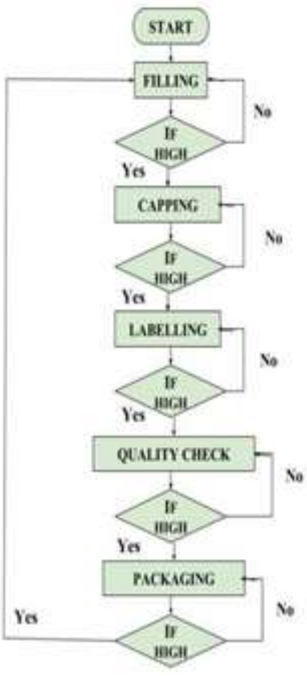

Fig5.1.Flowchartforautomaticbottlefillingcontroller

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Fig. 5.1definesthedifferent states of the controller, including IDLE,FILLING,CAPPING,LABELING,QUALITY_CHK, and PACKEGING. The`state`signal represents the current state of the controllerand is initialized to IDLE during reset. Inside theprocessblock,theFSMisimplementedusinga`case`statementbasedonthecurrentstate.Eachstatehasassociatedconditionsandactions:

5.2 Descriptionofstates:

IDLEstate: Thecontrollerwaitsforanemptybottletobedetected(`empty_sensor='1').Whenan emptybottleisdetected, theconveyorisactivated(`conveyor<='1'`),andthecontrollertransitions to theFILLINGstate.
FILLINGstate: Thevalveisturnedon(`valve <= '1'`)to fill thebottleuntil itbecomesfull(`full_sensor='1'`). Oncethebottleis full, thevalveis turnedoff, theconveyoris activated,andthecontrollertransitionsto theCAPPINGstate.
CAPPINGstate: Thecapperisactivated(`capper<='1'`)tocheckandtightenthebottlecap.Whenthecapisdetected(`cap_sensor='1'`),thecapperisturnedoff,theconveyorisactivated,andthecontrollertransitions totheLABELINGstate.Thelabelleris alsoactivated(`labeller<='1'`)inthis state.

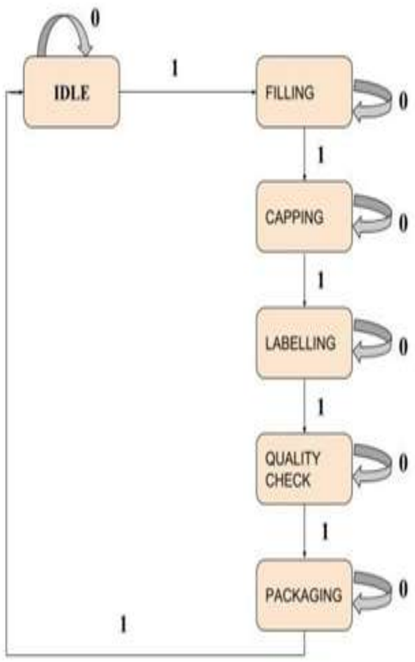


Fig5.2.Statediagramforautomaticbottlefillingcontroller.

LABELING state: Thelabel is appliedto thebottlewhen thelabelsensordetects thebottle(lable_sensor='1'`).Afterlabelling,thelabeleristurned off,theconveyorisactivated, andthecontrollertransitionstotheQUALITY_CHKstate.Thecheckingsignal(`cheking<='1'`)isactivatedin this state.

QUALITY_CHK state: Thequalityofthefilledbottleischecked(`quality_check='1'`).Ifthequalitycheckpasses,thecheckingsignalisturnedoff,theconveyorisactivated,andthecontrollertransitions tothePACKEGINGstate.

PACKAGINGstate: Thebottlesarepackaged(`packager<='1'`).Oncepackagingiscompleted(`packaging_done='1'`),thepackageristurnedoff,theconveyorisactivated,andthecontrollertransitions back totheIDLEstatetowaitforthenextempty bottle.
The code also includes default assignments for theoutput signals in the `others` state and during resettoensureproperinitializationanderrorhandling.
In summary, the code implements a bottle fillingcontroller FSM that controls the filling,capping,labeling, quality checking, and packaging processesof the automatic bottle filling plant. The controllertransitionsbetweenstatesbasedonspecificconditions and activates the necessary componentsto perform the corresponding actions at each stageofthebottlefilling process.

VI. SIMULATION AND TESTING:

The system is tested and simulated usingVivado software. The simulation results show thatthesystemisabletofillbottlesaccuratelyandefficiently.Thesystemisabletodetectthepresenceof bottles on the conveyor belt, fill the bottles withthespecified amount of liquid,andtransport thebottlesawayfromthefillingmachine.Thesystemisalso able to detect errors in the filling process andtakecorrectiveaction.

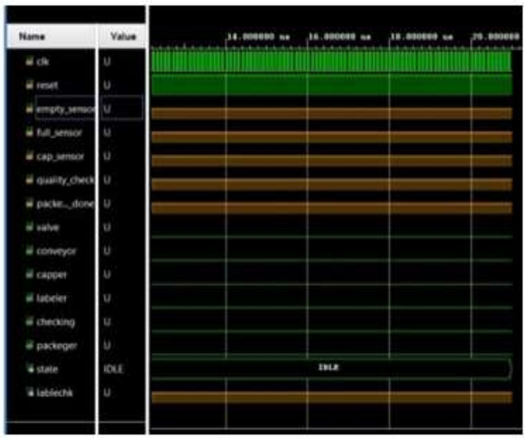


Fig5.1Simulationwaveform showingIdleState

The fig.5.1 shows the waveform of Idle State. When we give Clock signal and reset input to high the controller goes in Idle state all the outputs like Valve, Conveyor, capper etc. all goes Low (OFF) as per the VHDL code.

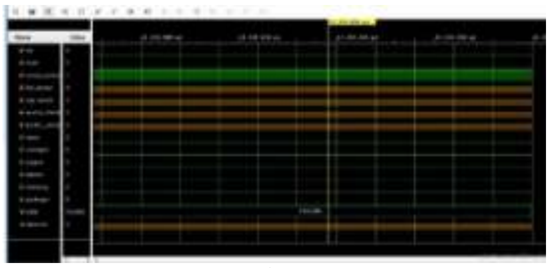


Fig5.2.SimulationwaveformshowingFillingState

The fig.5.2 shows the Simulation waveform of Filling State, When we give high input to empty bottle sensor (Empty bottle detected) then controller goes to Filling state, then Valve turns On (high) and filling of bottle starts.

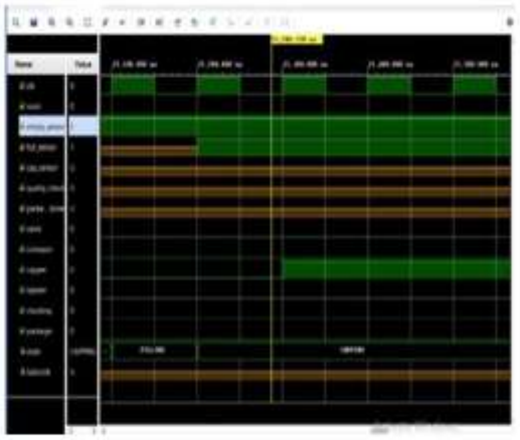


Fig 5.3SimulationwaveformshowingCappingState

The fig. 5.3 shows the Simulation waveform of Capping State, When we give high input to the bottle filled sensor (bottle is filled) then Valve turns OFF and the controller goes to Capping state, then Capper turns On (high) and Capping of bottle starts.

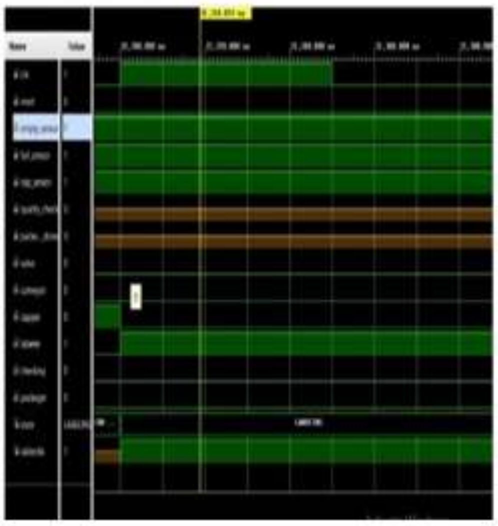


Fig 5.4Simulationwaveform showing LabellingState

The fig.5.4 shows the Simulation waveform of Capping State When we give high input to the Capping sensor (bottle is capped) then capper turns OFF and the controller goes to Labelling state, then Labeler turns ON and Labelling of bottle starts as per program.

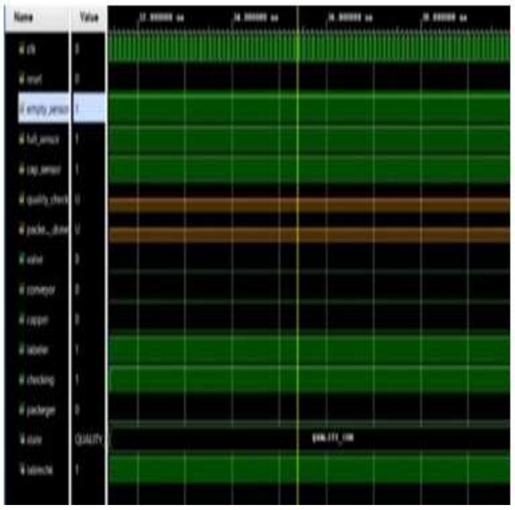


Fig 5.5Simulationwaveform showingQualityCheck State

The fig.5.5 shows the Simulation waveform of Capping State, When we give high input to the Labelling sensor (bottle is Labelled) then Labeler turns OFF and the controller goes to Quality Check state, then Quality Checking turns ON and Checking of bottle starts as per program.

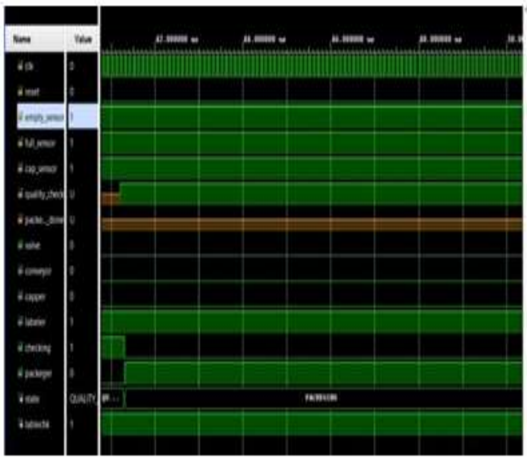


Fig 5.6 .Simulationwaveform showingPackagingState

The fig.5.6 shows the Simulation waveform of Packaging State When we give high input to the Quality check sensor (bottle Quality is checked) then Quality Checking turns OFF and the controller goes to Packaging state, then Packager turns ON and Packaging of bottle starts.

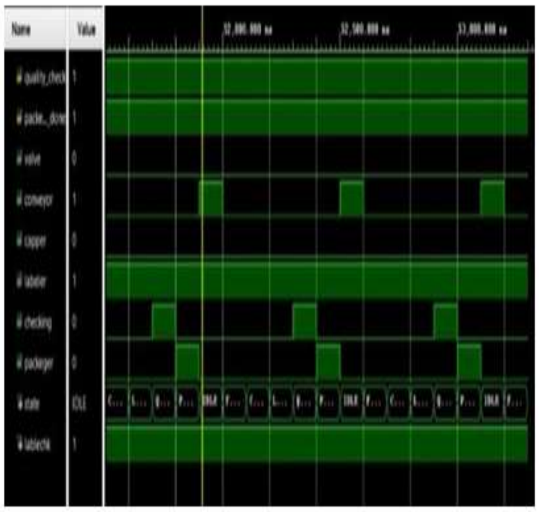


Fig 5.7. Simulation waveformForautomaticbottle filling Controller

The fig.5.7 shows the Simulation waveform of automatic bottle filling Controller, As per our VHDL
code controller shows the results from one state to another and so on, And this process achieves our aim to automate the bottle filling process by using FPGA.

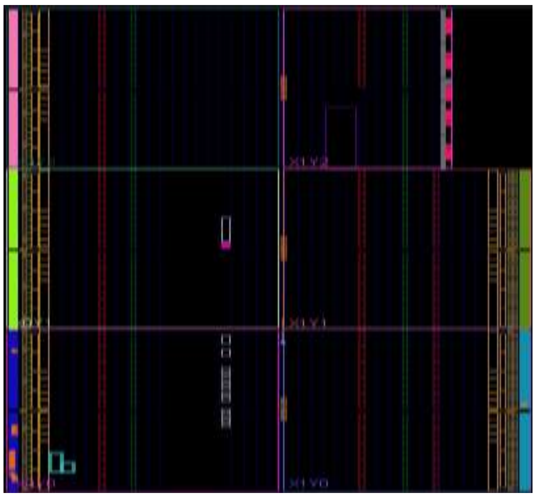


Fig 5.8 Implementation Design

Fig 5.8 shows theImplementation Designof the automatic bottle filling plant controller Using VHDL language. The automatic bottle filling plant controller consists of sensing systems to detect bottles and measure liquid levels. It controls the conveyor system for bottle transport and synchronizes the filling mechanism. The controller employs algorithms for precise control, adjusts conveyor speed, and manages the overall operation. It includes a user-friendly interface for monitoring and control, and a central unit for processing signals and coordinating components. Safety features and data logging for analysis are also incorporated.

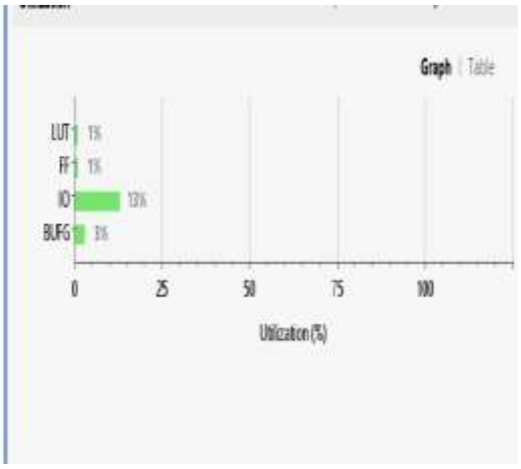
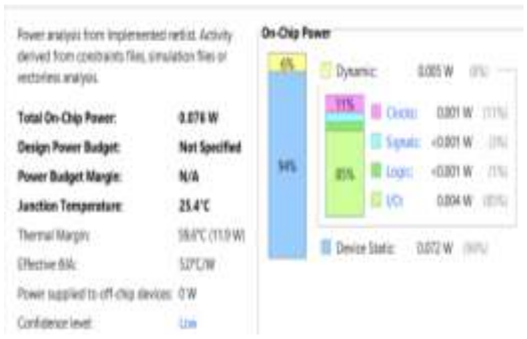


Fig.5.9 utilization graph

Above fig.5.9 is graph the utilization graph of the automatic bottle filling plant controller. An utilization graph represents resource allocation in a system over time. Designing an automatic bottle filling plant controller using VHDL involves identifying requirements, defining architecture, writing VHDL code, simulating and verifying, synthesizing and implementing, and performing utilization analysis.Optimization techniques include resource sharing, pipeline design, parallelization, and code optimization. Utilization graphs can be generated using VHDL simulation or synthesis tools with utilization analysis capabilities.



Power analysis from implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.076 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**25.4°C**
Thermal Margin:	59.6°C (11.9 W)
Effective θJA:	5.0°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

On-Chip Power

Dynamic:	0.005 W	(6%)
Clocks:	0.001 W	(11%)
Signals:	<0.001 W	(3%)
Logic:	<0.001 W	(1%)
I/O:	0.004 W	(85%)
Device Static:	0.072 W	(94%)

Fig 5.10 chip power

As we see in Fig 7.3, is a diagram is of chip power of FPGA. The chip power of an FPGA (Field-Programmable Gate Array) refers to the power consumption of the FPGA chip itself. It is an important consideration in FPGA design. Factors that influence chip power include the configuration of logic elements, memory elements, interconnects, and I/O interfaces. Power consumption can vary based on the specific FPGA model, the configuration of thedesign, and the operating conditions. Designers aim to optimize power usage through techniques such as power gating, clock gating, and voltage scaling. Power reports estimation tools andare available to analyze and optimize chip power in FPGA designs. TheRTLviewofthemachineisshowninfigure5.8
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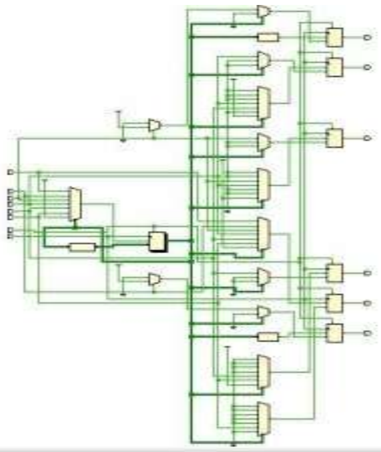

Fig 14. RTL view of Automatic bottle fillingController.

VII. CONCLUSION:

The present FPGA based automatic bottle fillingcontroller is implemented using FSMs with the helpofXilinxVivado.Thedesignisverifiedon theFPGA Basys 3 development Board. The VHDL-baseddesignprovidesaflexibleandscalablesolution that can be easily adapted to different typesof liquids and bottle sizes, making it applicable invarious industries. By utilizing a state diagram andappropriate input and output modules, the systemcan accurately detect and control the filling process,ensuringthateachbottleisfilledtothedesiredlevel. .The verification and synthesis of the VHDL code,followedbytheplacementandroutingofthedesignontotheFPGA,enablethesystemtobeimplementedandprogrammedeffectively.Thesimulation process ensures the correct functionalityofthesystem,whiletheFPGAimplementationallows forreal-world testingandvalidation.Overall,theimplementationoftheAutomaticBottleFillingControllerusingVHDLdemonstratesthepotential of digital circuit design and automation inenhancingindustrialprocesses.Thesuccessfulintegration of hardware and software componentspaves the way for improved efficiency, accuracy,and productivity in bottle filling operations, makingitavaluablecontribution tothefield.

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