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High Performance Design and Implemantion of DDR SDRAM Controller

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ABSTRACT: This controller is targeted at high bandwidth applications such as live video processing. It is designed to drive 256-bit DDR SDRAM memory. The DDR SDRAM architecture employs a 2n-prefetch architecture, where the internal data bus is twice the width of the external data bus. A single read or write cycle involves a single 2n-bit wide, one-clock-cycle data transfer at the core, and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O. Thus, this enables high-speed operation as the internal column accesses are half the frequency of the external data transfer rate. DDR SDRAMs use a byte-wide, bidirectional data strobe (DQS) that is transmitted externally, along with data (DQ) for data capture. DQS is transmitted edge-aligned by the DDR SDRAM during reads, and center-aligned by the controller during writes to the memory. The DDR SDRAM utilizes on-chip delay-locked loops (DLLs) to clock out DQS and corresponding DQs, ensuring that they are well matched and that they track each other with changes in voltage and temperature. For FPGA design the IC manufacturers are providing commercial memory controller IP cores working only on their products. Main disadvantage is the lack of memory access optimization for random memory access patterns. The 'data path' part of those controllers can be used free of charge. This work propose an architecture of a DDR SDRAM controller, which takes advantage of those available and well tested data paths and can be used for any FPGA device or ASIC design.

Keywords: Synchronous DRAM, Row Access Strobe, System-onchip, HPDMC, ModelSim, Xilinx ISE.

I. INTRODUCTION

The widening performance gap between processors and memory has made the memory subsystem one of the limiting factors of a general purpose computer system's performance. This phenomenon has been termed the Memory Wall. Modern memory systems usually have large bandwidths and this is often thought of as being able to compensate for large memory latencies. This may be true for applications where large data streams are used (such as media processing), but the availability of bandwidth alone cannot help to reduce all memory latencies. Because memory technologies are unlikely to change drastically in terms of their speed, more focus is usually put on changing the organization and interface of the memory to develop new memory designs. We are specially selecting memory type SDRAM as SDRAM and DDR memories are mostly used in memory designs of embedded systems as it is boosted with high speed, burst access, pipelining, portability and proper command initialization.

II. SYNCHRONOUS DRAM

Synchronous dynamic random access memory (SDRAM) is dynamic random access memory (DRAM) that is synchronized with the system bus. Classic DRAM has an asynchronous interface, which means that it responds as quickly as possible to changes in control inputs. SDRAM has a synchronous interface, meaning that it waits for a clock signal before responding to control inputs and is therefore synchronized with the computer's system bus enabling higher speed. The SDRAM controller is capable of either 16-bit or 32-bit data path, and supports byte, half-word and word access. Bursts can be used for both write and read access. A bidirectional data strobe (DQS) is

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transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR SDRAM during Reads and by the memory controller during Writes. DQS is edge-aligned with data for Reads and canter-aligned with data for Writes. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be accessed. The address bits registered coincident with the Read or Write command are used to select the bank and the starting column location for the burst access. The DDR SDRAM provides for programmable Read or Write burst lengths of 2, 4 or 8 locations. An Auto Precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access. As with standard SDRAMs, the pipelined, multibank architecture of DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

III. PROPOSED DDR SDRAM CONTROLLER

DDR SDRAM DESIGN FEATURES

- FIFO backend user interface
- Programmable burst lengths of 2, 4, 8, or full-page (available only in certain DRAMs)
- Programmable CAS latency of 2 and 3
- Burst length applies to both Read and Write cycles
- Interfaces with the DDR SDRAM at 200 MHz, DDR (400 Mb/s)
- Uses DQS to receive data from the memory

ARCHITECTURE OF HPDMC

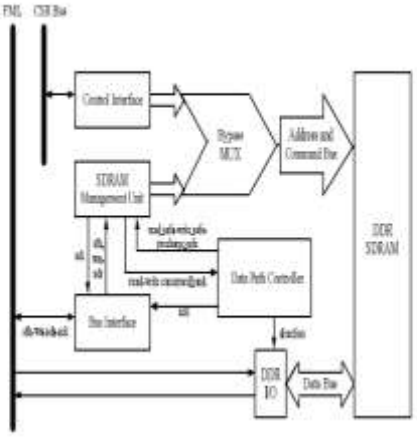

Fig.1: Block-diagram of proposed high performance SDRAM Controller.

HPDMC provides high flexibility and savings on hardware by implementing a bypass mode which gives the CPU low-level access to the SDRAM command interface (address pins, bank address pins, and CKE, CS, WE, CAS and RAS). The SDRAM initialization sequence is assigned to the CPU, which should use this mode to implement it. Timing parameters are also configurable at runtime.

Control interface

The control interface provides a register bank on a low-speed dedicated CSR bus, which is used to control the operating mode of the core, set timings, and initialize the SDRAM. The interface can access directly the SDRAM address and command bus in the so-called bypass mode. In this mode, the memory controller is disabled and the CPU can control each pin of the SDRAM control bus through the bypass register. This mode should be used at system boot-up to perform the SDRAM initialization sequence. HPDMC does not provide a hardware state machine that does such initialization.

SDRAM MANAGEMENT UNIT

The SDRAM management unit is a state machine which controls sequentially the SDRAM address and command bus. Unless the core is in bypass mode, the management unit has full control over the SDRAM bus. This unit is responsible forprecharging banks, activating rows, periodically refreshing the DRAM, and sending read and write commands to the SDRAM.

DATA PATH CONTROLLER

The data path controller is responsible for •Deciding the direction of the DQ and DQS pins • Delaying read, write and precharge commands from the management unit.

BUS INTERFACE

The bus interface is responsible for sending commands to the SDRAM management unit according to the request coming from the FML, and acknowledging bus cycles at the appropriate time. Fast Memory Link (FML) bus features • Synchronism. The bus is meant to be used in FPGA-based devices, whose architectures are designed for synchronous (clock-driven) systems. • • Burst oriented. Each cycle begins with an address phase, which is then followed by several data chunks which are transferred on consecutive clock edges (the data phase). The length of the burst is fixed. • Pipelined transfers. During the data phase of a cycle, the control lines are free and can

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be used to initiate the address phase of the next cycle.

FIFO (FIRST-IN FIRST-OUT)

To support the fast response time, burst mode access and read FIFO techniques need to be used whenever possible. When FML bus needs to read data, see if data is already in read FIFO by only checking if the current accessing address is in the range of either of the read FIFO and if the corresponding bit in the corresponding Valid-Vector is valid. The Valid-Vector is used to mark if the data stored in data FIFO is valid. Valid-Vector works like tags for a cache. Every read FIFO is only as big as the capacity of a SDRAM burst, so that Valid-Vector is only a several bit vector. If the needed data is in read FIFO, data can be directly read from them, otherwise, a READ command is needed issuing to SDRAM. After a pre-set number of clock cycles, the data is available on the output latches of the SDRAM for reading, and data is delivered to FML bus and written to one of the read FIFO at the same time. The whole burst access data will be loaded in read FIFO.

Table 1: Comparison between DDR2 and DDR3

	DDR2 SDRAM	DDR3 SDRAM
Data transfer rate	400-800Mbits/s	800-1600Mbits/s
Voltage	1.8 V±0.1V	1.5V±0.075V
Banks	4/8	8
Prefetch	4 bits	8 bits
Burst Length	BL= 4,8	BL =4,8
Topology	Conventional T	Fly-by
Chips packaging	60 BGA for×4/×8	78 BGA for×4/×8
	84 BGA for×16	96 BGA for×16
Chips capacity	256 Mbit -4Gbit	512 Mbit -8Gbit

the architecture of DDR3SDRAM controller consists mainly consists of write data FIFO, read data FIFO reg, address FIFO, Command_FIFO, clock counter and refresh counter, initialization_fsm, command_fsm, data path, bank control. To initialize the modules present in the design architecture by using initialization_fsm signal this propagates proper i-state to perform particular action. And to perform the normal read write, high write and high read operations by using command_fsm signal, this propagates c-state forparticular action. Data latching and data dispatching is done by using data path modules from external circuit unit to memory banks of DDR3 SDRAM vice versa. To open the exact bank and exact address location in that bank, here the DDR3 SDRAM bank management system uses the address FIFO, this gives an address to the command_fsm so that the bank control unit can do this particular operation. the Write data FIFO provides the data to the data path module In the case of normal write and fast write operation. The read data reg gets the data from the data path module normal and high read operation. The DDR3 controller gets the address, data and control from the external circuit in to the Address FIFO. Write data FIFO and control FIFO respectively.

IV. PROGRAMMING AND RESULTS

When the system is powered up, HPDMC comes up in bypass mode and the SDRAM initialization sequence should be performed from then, by controlling the pins at a low level using the bypass register. The SDRAM must be programmed to use a fixed burst length of 8, and a CAS latency of 2 (preferred) or 3, CAS latency 2.5 is not supported.the snapshots of the simulation results of DDR3 controller in various modes of operation. Simulation and synthesis of the design is done by using “Verilog HDL” language in Xilinx virtex 5 FPGA XC5 VLX50T+ 113 series kit.

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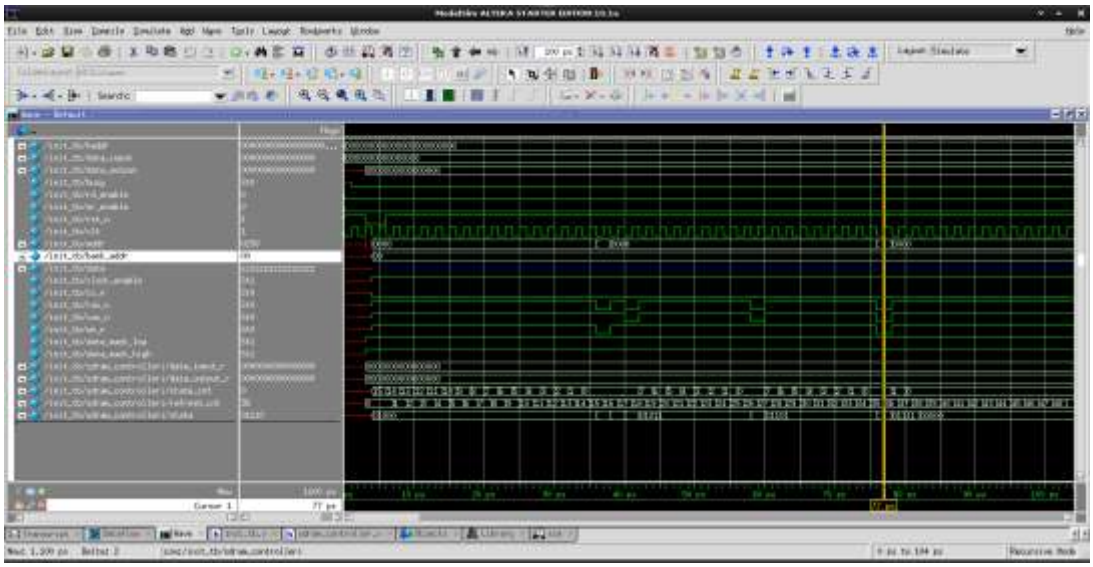

FIG2: RESULTS OF SIMULATION IN REFRESH LOGIC MODE.

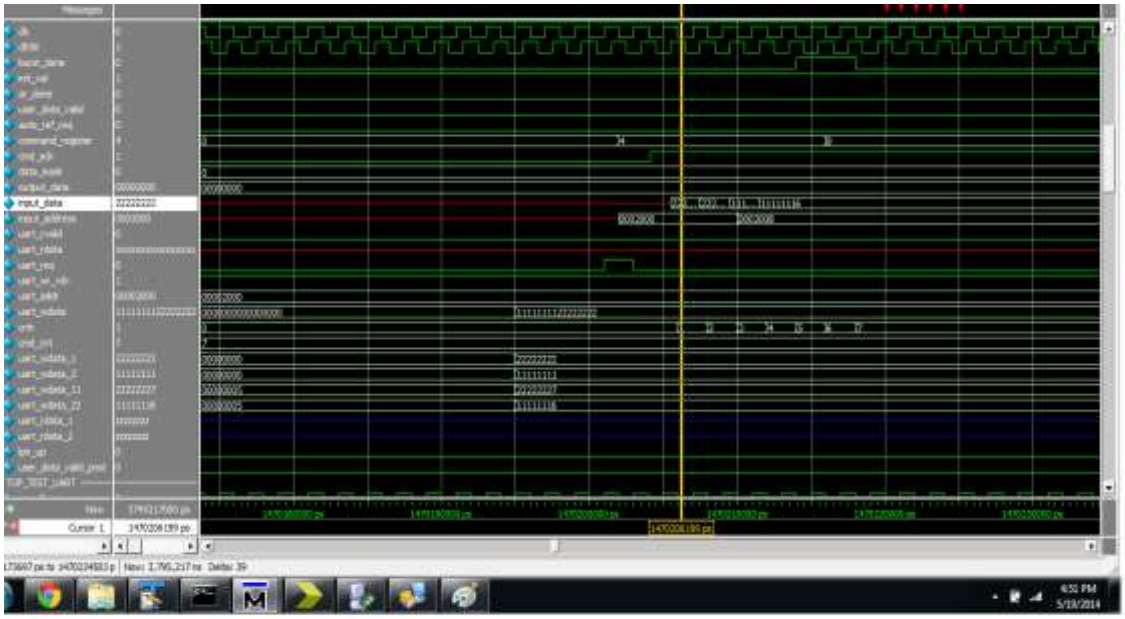

FIG3: RESULTS OF SIMULATION IN WRITE MODE.

COMPRESSION TABLE

Parameters	Existing Model	Proposed Model
Power Supply	1.8 ± 0.1 V	1.7 ± 0.1 V
Area	29mm	27mm
Delay	2.5ns	2.4ns
Gate Count	64 million transistor	68 million transistor

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V. CONCLUSION AND FUTURE SCOPE

The results of the experimentation using a realistic description of a hardware design have revealed some insights into the performance of a DDR SDRAM memory system and the controller used in such a system. First, some general observations about SDRAM-based memory can be made.high performance DDR3 SDRAM memory controller for computing system using virtex 5 FPGA XC5 was designed and implemented. DDR3 SDRAM controller gives adequate hardware and software compatibility to provide efficient code for offload applications to get advantages of high bandwidth and fast performance on switching operation from the storage array. DDR3 SDRAM controller is designed using system Verilog simulation and synthesis is done by using Xilinx Virtex 5 FPGA XC5 VLX50T+ 1136 series kit. Using XPower analyzer tool, here the tool will analyzed the dynamic power consumptions and power leakage in the circuit. DDR3 SDRAM devices runs at 1.5V and achieves high speed operations.DDR3 memory devices are reduces 30% of power consumption compared to DDR2. By using DDR3 SDRAM controller architecture we can reduce power from 0.080W to 0.077W and also it improves heat generation, gives high memory configurations for storing higher capacity of data. These observations, coupled with the novel contributions of this work, can indicate where future work in the field should be done to further improve the performance of the memory system, decreasing the memory access time, power and area. The constant need to boost memory performance for increasingly powerful system processors drives the development of advanced memory technologies.

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