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Implementation of Low Power High Speed Alu by Using Reversible Logical Gates

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ABSTRACT: In current scenario, the reversible logic design attracting more interest due to its low power consumption. Reversible logic is very important in low-power circuit design. The important reversible gates used for reversible logic synthesis are Feynman Gate, Fredkin gate, toffoli gate etc. This paper present a basic reversible gate to build more complicated circuits which can be implemented in ALU, some sequential circuits as well as in some combinational circuits. It also gives brief idea to build adder circuits using the basic reversible gate like peres gate this paper proposes a novel 4x4 bit reversible fault tolerant multiplier circuit which can multiply two 4-bit numbers. This based on two concepts. The partial products can be generated in parallel using PG gates and thereafter the addition is done by using reversible parallel adder designed from PFAG gates. Thus, this paper provides idea for building of more complex system which can execute more complicated operations using reversible logic.

Index Terms— Keywords - Garbage output, peres gate, PFAG, Reversible logic

I. INTRODUCTION

Energy dissipation is an important consideration in VLSI design. Reversible logic was first related to energy when Landauer states that information loss due to function irreversibility leads to energy dissipation. This principle is further supported by Bennett that zero energy dissipation can be achieved only when the circuit contains reversible gates [2].Information is lost when the input vector cannot be uniquely recovered from its output vectors. Reversible logic circuits naturally take care of heating since in a reversible logic every input vector can be uniquely recovered from its output vectors and therefore no information is lost. According to [1,2] zero energy dissipation would be possible only if the network consists of reversible gates. Thus reversibility will become an essential property in future circuit design. Reversible circuits are also interesting because the loss of bits of information implies energy loss. However, reversible logic is suffering from two problems. Firstly, there is a lack of technologies with which to build reversible gates. Work is certainly continuing in this area. Secondly, while there is much research into how to design combinational circuits using reversible logic, there is little in the area of sequential reversible logic implementations. . "To establish the relevance of reversible and quantum computing it seems appropriate to note that the VLSI industry is moving at high speed towards miniaturization. With miniaturization it faces two issues: i) A considerable amount of energy gets dissipated in VLSI circuits and ii) the size of the transistors are approaching the quantum limits where tunneling and other quantum phenomena are likely to appear. Thus, we need a superior technology that can circumvent these problems.Power dissipation is one of the important parameters in the digital circuit design. In VLSI circuit designing where power dissipation plays an important role, there has been an increasing trend of packing more and more logic elements into smaller and smaller volumes and clocking them with higher frequencies. The logic elements are normally irreversible in nature and according to Landauer's principle irreversible logic computation results in energy dissipation due to power loss. This is because; erasure of each bit of information dissipates at least KTln2 Joules of energy where K is Boltzamann's constant and T is the absolute temperature at which the operation is

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performed. By 2020 this will become a substantial part of energy dissipation, if Moore's law continues to be in effect which states that processing power will double every 18 months. This particular problem of VLSI designing was realized by Feynman and Bennet in 1970s. In 1973 Bennet [2] had shown that energy dissipation problem of VLSI circuits can be circumvented by using reversible logic. This is so because reversible computation does not require erasing any bit of information and consequently it does not dissipate any energy for computation. . In a short period the reversible computation has emerged as a promising technology having applications in low power CMOS, nanotechnology ,optical computing ,optical information processing, DNA computing, bioinformatics, digital signal processing and quantum computing. It is very clear that reversible circuits will play dominant role in future technologies. These facts motivated many researchers to work in this domain A reversible logic gate must have the same number of inputs and outputs, and for each input pattern there must be a unique output pattern. Thus, Reversible logic circuits avoid energy loss by un computing the computed information by recycling the energy in the system. In the design of reversible circuits two restrictions should be considered; firstly, Fan-out is not permitted and secondly, Feedback from gate outputs to inputs is not permitted. Due to these restrictions, synthesis of reversible circuits can be carried out from the inputs towards the outputs and vice versa . So, there is a one-to-one mapping between input and output vector. A logic synthesis technique using a reversible gate should have the features like minimum gate count along with less use of constants and garbage generation. Reduction of these parameters is the main design focus. Reversible circuits for different purposes like half adder, full adder multiplier[3-11,15] have been proposed recently. Among these reversible circuits, multiplier circuits are of special importance because of the fact that they are the integral components of every computer system, cellular phone and most digital audio/video devices.

II. LITERATURE SURVEY

PawelKerntopf [20] explained multipurpose Reversible gates and example of efficient binary multipurpose reversible gates. Thapliyal and Ranganathan [5] proposed the design of Reversible Binary Sub tractor using TR Gate. The particular function like Binary Subtraction is implemented using TR gate effectively by reducing number of Reversible gates, Garbage outputs and Quantum Cost.

Thapliyal and Ranganathan [6] presented a design of Reversible latches viz., D Latch, JK latch, T latch and SR latch that are optimized in terms of quantum cost, delay and garbage outputs. Lihui Ni et al., [7] described general approach to construct the Reversible full adder and can be extended to a variety of Reversible full-adders with only two Reversible gates.

Irina Hashmi and Hafiz HasanBabu [8] designed an efficient reversible barrel shifter which is capable of left shift/rotate used for high speed ALU applications. Robert Wille et al., [9] explored two techniques from irreversible equivalence checking applied in the reversible circuit domain. (i) Decision diagram Technique equivalence checking for quantum circuits and (ii) Boolean satifiability checking for garbage input/outputs. Noor MuhammedNayeem et al., [10] presented designs of Reversible shift registers such as serial-in serial-out, serial-in parallel-out, parallel-in serialout, parallel-in parallel-out and universal shift registers. Majid Mohammadi, Mohammad Eshghi et al., [11] proposed a synthesis method to realize a Reversible Binary Coded Decimal adder/subtractor circuit. Genetic algorithms and don't care concepts used to design and optimize all parts of a Binary Coded Decimal adder circuit in terms of number of garbage inputs/outputs and quantum cost. Majid Mohammadi and Mohammad Eshghi [12] explained about the behavioral description and synthesis of quantum gates. To synthesize reversible logic circuits, V and V+ gates are shown in the truth table form and shown that bigger circuits with more number of gates can be synthesized. Rekha James et al.,[13] proposed an implementation of Binary Coded Decimal adder in Reversible logic, which is basis of ALU for reversible CPU. VLSI implementations using one type of building block can decrease system design and manufacturing cost. HimanshuThapliyaland Vinod [14] presented the Transistor realization of a new 4*4 Reversible TSG gate. The gate alone operates as a Reversible full adder.

The Transistor realizations of 1-bit Reversible full adder, ripple carry adder and carry skip adder are also discussed. HimanshuThapliyal and Srinivas [15] proposed a 3x3 Reversible TKS gate with two of its outputs working as 2:1 multiplexer. The gate used to design a Reversible half adder and further used to design multiplexer based Reversible full adder. The multiplexer based full adder is further used to design Reversible 4x4 Array and modified Baugh Woolley multipliers Yvan Van Rentergem and Alexis De Vos [16] presented four designs for Reversible full-adder circuits and the implementation of these logic

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circuits into electronic circuitry based on C-MOS technology and pass-transistor design. The chip containing three different Reversible full adders are discussed. Mozammel Khan [17] proposed realizations of ternary half and full-adder circuits using generalized ternary gates. Mozammel Khan [18] discussed quantum realization of ternary Toffoli gate which requires fewer gates than the existing literature. Abhinav Agrawal and NirajJha [19] presented 6 the first practical synthesis algorithm and tool for Reversible functions with a large number of inputs. It uses positive-polarity Reed-Muller decomposition at each stage to synthesize the function as a network.

III. EXISTTING METHODOLOGY

The Sir Bernard Law solution for modular duplication is known as the fastest series of rules to measure xy mod n in computer systems when the values of x, y and n are massive. Within this lecture, we will define the Montgomery series of modular multiplication policies. This is one of the algorithm information that my college students had difficulty apprehending.

Montgomery Multiplication is a method for wearing lots quicker compact replicate of major cryptographic sets. Bernard Law Sir Bernard Law arithmetic is a compact replica calculator in which a, b and moreover n declare integers[2] Bernard Law Sir Bernard Law gadgets turns proper numbers right into a website named 1st viscount Montgomery of alamein region as well as includes critical operations and returned converts which eliminates the need of more division t The steps concerned about Sir Bernard Law Multiplication are:

1. Consider two integers a and b less than modulo n

2. Introduce a number R greater than n such that gcd (R, N) =1

3. Find two integers R-1and N-1 such that: RR-1-NN-1 =1.

4. Transform the multipliers to Montgomery space by the following multiplication and reduction:

$$A=a\times R \bmod N$$

$$B=b\times R \bmod N.$$

5. Compute the Montgomery multiplication using the algorithm in Figure 1 which computes product of A and B giving the result S in Montgomery space that is

$$S=A\times B\times R\text{-}1 \bmod N$$

6. The final result can be obtained by back transforming from Montgomery space:

$$s=S\times R\text{-}1 \bmod N.$$

The rationale behind this computation is to find a proper value of q so that, at the k-th iteration, the value of $A + xkY + qN$ is a multiple of β. and that this value is bounded by $(R + \beta k)N$. As explained above, the value of q i

$$q = (A + xkY)N\ 0 \bmod \beta,$$

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Montgomery Algorithm:

Function

montgomery (X, Y)

Begin

A: = 0;

For k : = 0 to m − 1 do begin

q: = (a0 + xky0)(β − n0) −1 β
mod β; A := A + xkY + qN;

A: = A/β; end;

Return A;

End.

In this process, the high-priced branch machine typically used for compact bargaining is modified by way of clean trade methods by translating the operands into the name of the RNS area prior to service and retransforming the result after technique. A radix R is selected to be 2 extra than one word size and also extra than the node, i.e. R= 2w M. To be relatively immoderate, the collection of rules to include R identical to M, i.e. should have no odd non-trivial divisors. With R third power, it's easily pleased to settle on an odd board. This moreover fits properly with the cryptographic scheme we're concentrating on, in which the eigenvalues is each a top normally nonsensical but 2or the element of two primes and, moreover, because of this weird as cool. RNS integer representations are pointed to as M compounds and are typically denominated as the integer component calls a bar over it. An integer a is properly modified into its equivalent M-residue by increasing it through R and also rising M-module. The re-transformation is done in another smooth design by separating the residue through R modulo M.

Everything framework supplied in the previous region is using Verilog HDL and synthesized using Synopsys Software compiler. Implementation details on simulation results occurs in this portion.

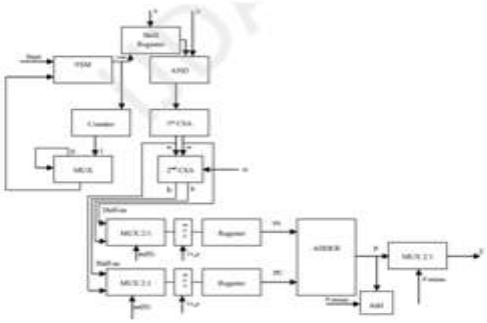

Fig.3.1 Proposed system architecture.

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Testing a complicated electronic interface math pattern poses a particular challenge to the exam bench clothier. Obviously, the research types to be generated can not be purely random variables, however they need considerable expertise in computing this. Consequently, next to join, take a good look at types, the corresponding final results variables for assessment.

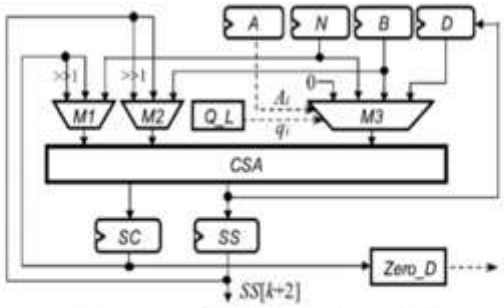

Fig. 3.2 Diagram of Montgomery Modular Multiplier.

Along with the right really worth the details, understanding the clock period when it reaches or exits the circuit is also utterly crucial. The framework involves millions of phases of logic or intermediary signs on rates; as a result, the end result of tests no longer correlates consistently with the exam vector middle. Useful testing does not find the only major path delays a model has. The critical path survival at once relates the first-rate frequency of the clock a system should maintain which would be identified at the point of synthesis.

Disadvantages:

- Not provided the output with Chr
- More Area, and Power
- Low Performance

IV. PROPOSED SYSTEM

A logic synthesis technique using a reversible gate should have the features like minimum gate count along with less use of constants and garbage generation. Reduction of these parameters is the main design focus. It is important for every processor to have a high speed multiplier. The design of the multiplier is based on parallel operation .it is done using two steps. Part i: Partial Product Generation (PPG) Part ii: Reversible Fault Tolerant Parallel Adder (RFTPA) As mentioned before, the purpose of this paper is the design of reversible fault tolerant multiplier circuit with the aim of optimizing its hardware complexity to make it more economical in terms of number of garbage outputs and constant inputs without losing its efficiency. The multiplier is implemented using PG and PFAG gates. The operation of a 4*4 reversible multiplier in Fig1. It consists of 16 Partial product bits of the four bit inputs X and Y to perform 4 * 4 multiplications.

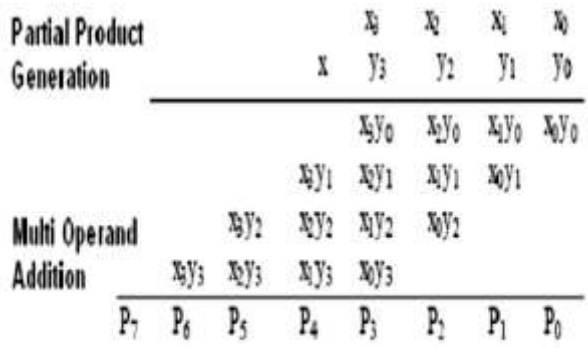

Fig 1. Basic 4*4 multiplication

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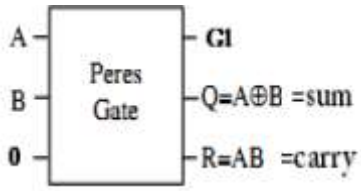

Fig 2. PG Gate as half adder

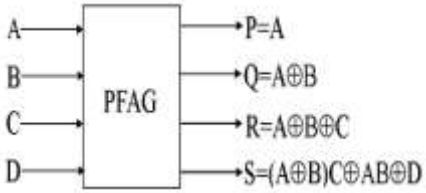

Fig 3. PFAG gate for full adder addition

PG gate used as half adder is shown in Fig.2. It requires one constant inputs of logic 0 and produces the required sum and carry term with one garbage outputs. To implement full adder circuit we can use PFAG gate as shown in fig.3.

PARTIAL PRODUCT GENERATION (PPG)

For product term generation the PG gate is used. The PG gate is used to perform AND operation by forcing one constant input as logic 0 whereas it produces required product term along with two garbage outputs. The Fig. 4 shows the implementation of AND operation using PG Multiplier partial products are generated using 16 PG gates as shown in Fig. 4.

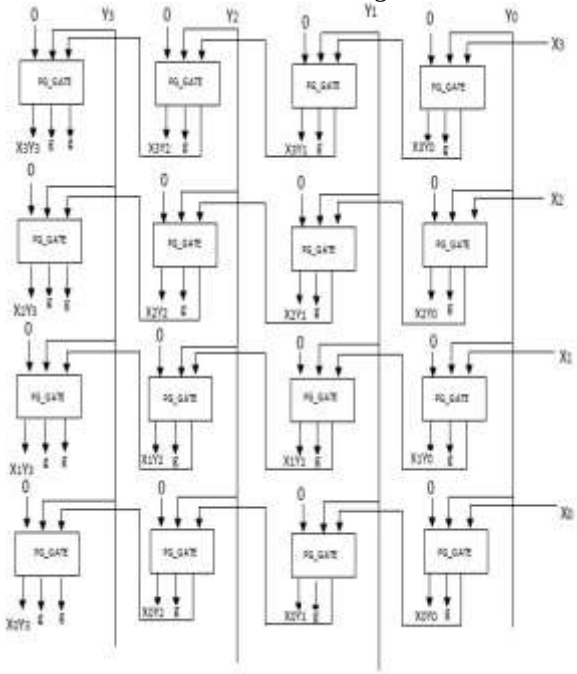

FIG 4. PPG using PG gate

Reversible Fault Tolerant Parallel Adder (RFTPA)

The RFTPA circuit needs reversible fault tolerant full adder (FTFA) and half adder (FTHA). Many reversible full adders have been proposed in the past. For example, TSG, MKG,IG and HNG gates can singly perform the full adder operation. Design of multipliers with these gates indicates the different critical parameters for reversible multipliers.Experimental results of different reversible multiplier circuits in terms of number of garbage outputs and constant inputs show that

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multiplier circuits with adders designed using PFAG gates have better results than multiplier circuits with PFAG gates.

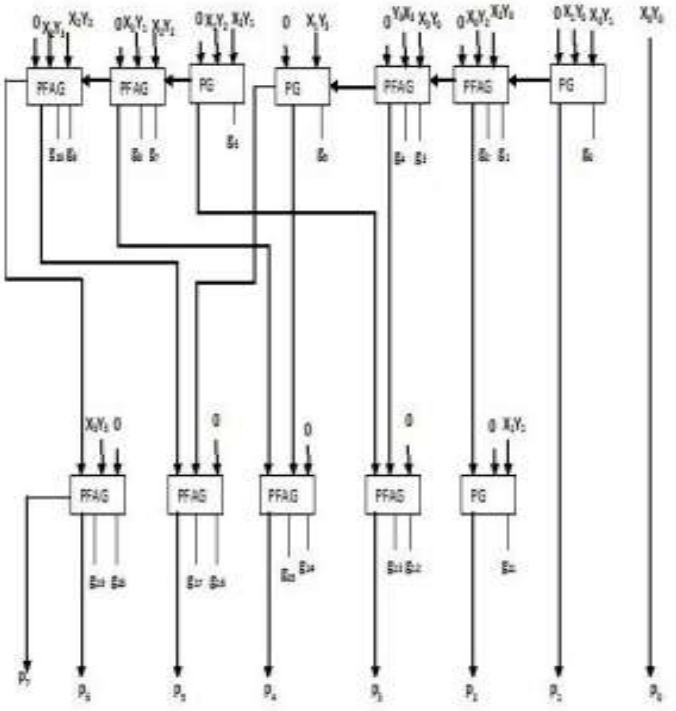
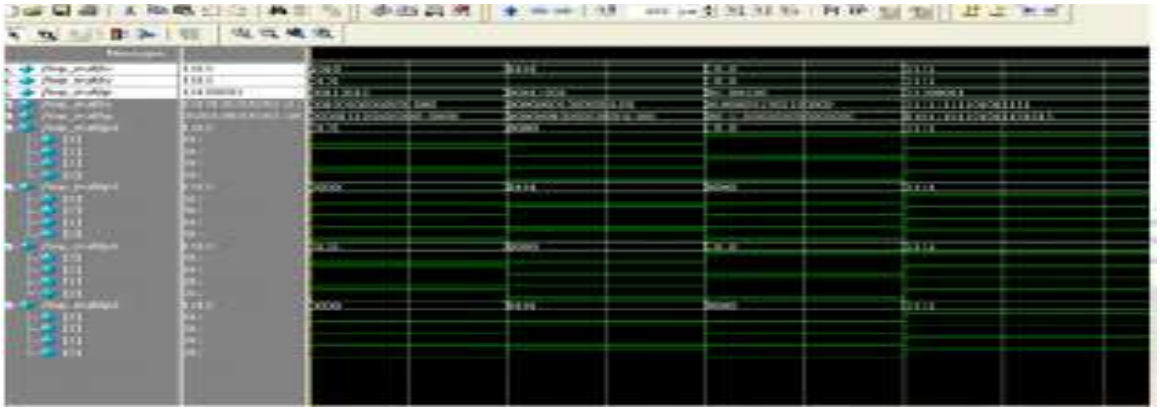


Fig.5 RFTPA Circuit

V. RESULTS

Different blocks of proposed system are designed coded in VERILOG HDL, simulated in I simulator and Xilinx ISE is the software tool used for FPGA synthesis.

SIMULATION RESULTS



RTL BLOCK DIAGARAM

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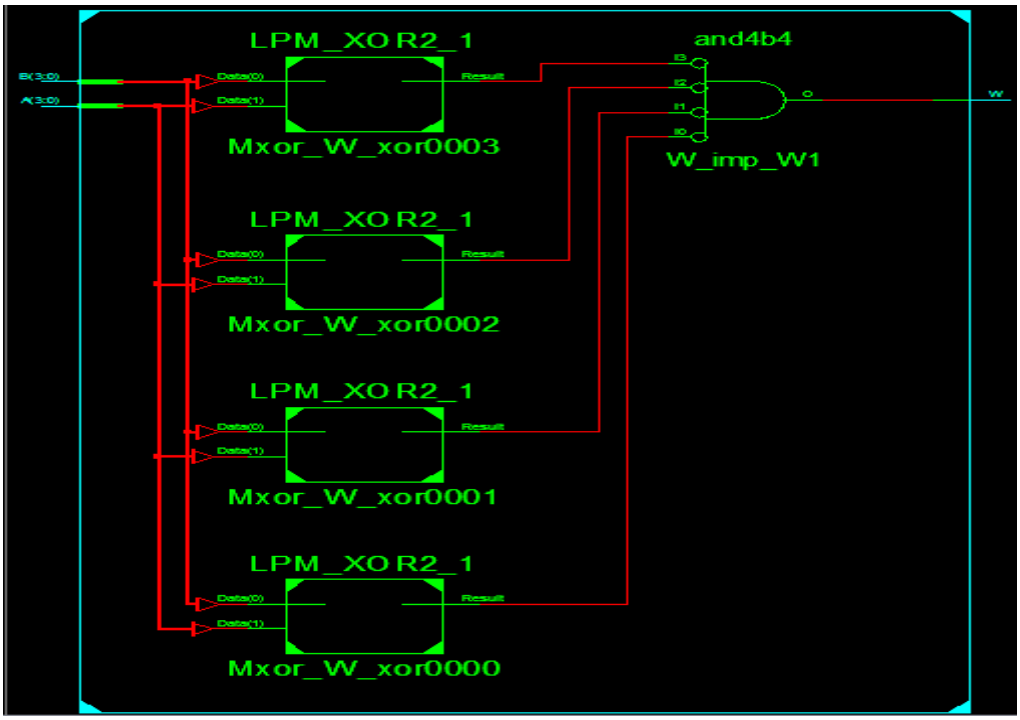

Table 1: Comparison Table for 4*4 Multiplier

Performance Parameter Spartan 3E	Reversible Multiplier TSG (2006)	Reversible Multiplier MKG (2008)	Proposed Fault Tolerant Reversible Multiplier
Gate Count	53	52	44
Constant input	58	56	56
Garbage	58	56	56

VI. CONCLUSION

Multiplier is a basic arithmetic cell in computer arithmetic units. The energy consumption in computation turns out to be deeply linked to the reversibility of the computation In the proposed work , we designed a reversible multiplier using pg and pfag gate with reduced gate count and reduced garbage output. The comparison table shows clear idea of the system with the existing one. Reduction in number of gate can reduce the circuit complexity . The chance for further research includes the reversible implementation of more complex arithmetic circuits such as function evaluation and multiplicative division circuits using this multiplier.

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