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Role of UPF and automation in low power checks and static verification

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ABSTRACT—Low Power devices are emerging at a very rapid rate as a lot of development is being carried out in this field. The need for these devices is increasing day by day, so more research is being done due to the high demand for such chips. RTL file alone is not able to take care of the power specifications of a device alone so there is a need for the introduction of a power-specific file that consists of all information and components of power. This file is called UPF file without which the design flow cannot function, at every stage this file is required and incremented according to the changes happening in the design as per specifications. A golden UPF or a reference file is written first. After writing UPF file then low power checks are done which make sure that the domains and cells placed between them get proper supply for the whole design to work properly and there are no floating values. Low power checks will make sure whether the strategies used are valid or not. If any special cell is placed, then whether it is getting proper supplies or not. Similarly static verification is needed to merge both the UPF and RTL files after elaboration so that simulations can be performed on it. Many power-saving techniques like multi-voltage, clock gating and power gating can be used to save a lot of power.

Keywords—UPF; power domain; low power; VC LP; level shifter; isolation cell; scripting; power state table;

I. INTRODUCTION

Low-power devices are in huge demand these days due to less area and better performance parameters. There is a need for research in this domain as when electronic devices startedprevailing to till now the size of devices has drastically reduced while performance has drastically increased.It was beyond imagination at a certain time in the past to even think of having such devices which would connect us anywhere in this world. Initially resources were limited and hence innovation took place in that specified range. As people started to research in this field, eventually many devices started coming into the picture and the main objective of such devices was the same i.e.improving performance while reducing the power it took.[10]This objective led to many great discoveries and hence in the industry there is a great demand for low-power devices today. This work revolves around low power checks along with static verification of a design. The VLSI design flow is such that the RTL information is readily available but not the information about voltages and hence power which does not give flexibility to alter it according to the user's requirements. This is when a standard like UPF came into picture and the whole scenario changed. UPF file takes the basic components of power into account and writes it in form of a script which is altered at every stage of design flow according to the requirements of the user. Alternatively, low-power checks are required to check if the inter-domain signal crossing is proper as well as the special cells like retention cells are properly placed to support the functionality ofthe low power design. Moreover, to accompany low power checks static verification is performed to verify the design functionality.[13]

II. UPF

As the advancements in low power technologies is taking place rapidly, there is a rapid need to introduce a particular standard that can be uniformly accepted everywhere. This need was taken care of by the introduction of writing a power

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file, that contained only the information related to the power of that device. Usually, a power file is not written before and simply RTL simulation is carried out, but it has a very major gap as low power cannot be catered to without power intent information. At every level of design flow, this file is required and is updated according to the results of that stage. Gate length reduction with the advancement of chips in modern days leads to increased power consumption, UPF file plays a very crucial role here due to its flexibility and ease of writing. It contains information about the power domains, and various types of cells that are required for catering operations such as shifting from one domain to another with different voltage levels or isolating a domain from others if its functionality is to turn off after some time. It is named as it contains a union of all the components required for representing a power file and incrementing it according to the stage it is in. Power verification is also very crucial as it takes a lot of time if the special cells like retention cells, level shifter cells are not placed properly. Also, the number of power domains plays an important role as their equivalence can lead to a reduction of power domains and hence lead to low power consumption.[1]

A. Power Domain

The main component of a UPF file is a power domain which contains information about the power supply and the supply nets and sets associated with it. A scope is usually defined while creating a power domain and it talks about the current design on which work is going on. It will include everything which will be below it as well. It is the first component of a UPF file and its definition tells about the major components of design. As its name suggests it defines a domain that contains all the power related useful data. PD represents a power domain and there are three power domains in the figure below.[5]

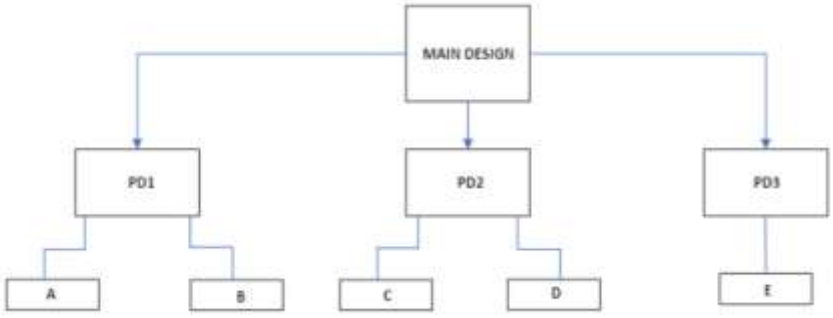

Fig 1:- Power domain structure

The main power domain includes all the elements beneath it, defined by the scope.

create_power_domainPD_Main_Design -include scope

If another case is taken into the picture where a new power domain called PD1 is to be created according to the specifications of the design then the same command will be used and its elements will be included automatically.[8]

create_power_domain PD_PD1 -elements {PD1}

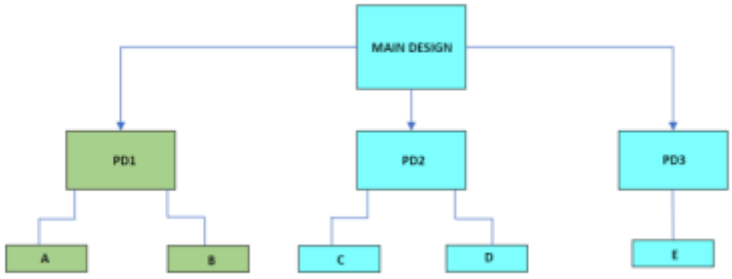

Fig 2 :- Creation of another power domain PD1

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B. Sypply nets and ports

Once the power domain is set, then comes supply ports and nets used to design the power networks. The voltage supply is transported to the power domain with the help of a supply port and supply nets. The supply port connects the power domain and supply net. They act like connecting bridges and dots between different components and power domains. If power domain is the base, supply nets and port form the basic interconnecting channels. In general, connecting point for nets is power supply and nets are descriptions of power network. In short, they are very important part for a power intent file.[4]

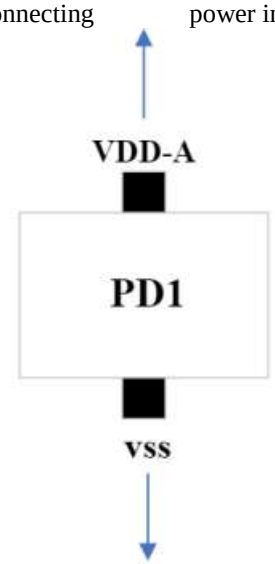

Fig 3:- Supply net and port

create_supply_net VDD_A -domain PD_PD1
create_supply_port VDD_A -domain PD_PD1 -direction <in/out/inout>

After the creation of both supply nets and ports, now they need to be connected. Similar command connecting them is written after creating them.[3, 13]

connect_supply_net VDD_A -ports VDD_A

C. Supply sets

Supply sets can alternatively be used in place of supply nets and ports. A total of three files are created with the power domain, primary file, default isolation, and default retention. The primary file contains power and ground information so while its creation there is no need to know the name of the power supply. They were added from UPF 2.0 onwards. The use of a supply set is such that it can help in getting the number of power domains down as similar groups of nets can be grouped together. Three functions are specified along with the command which defines the power, ground, and nwell/pwell type connections. The syntax of commands is as follows:
create_supply_set SET1 – function {POWER1} -function {GND} -function {nwell/pwell}

D. Power Switch

A power switch is required in the power intent file to control the amount of current entering a domain. The switch works under two conditions which are either on or off and are shown by 1 (ON) and a 0 (OFF). If the switch operates under on condition, it lets the current pass through the domains otherwise it stops the current from passing.[14]

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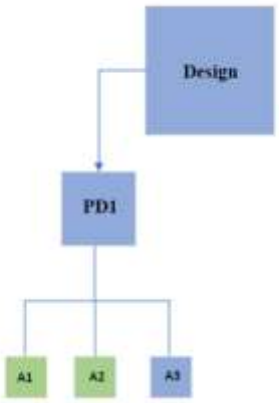

Fig 4:- Power domain

There are two power domains defined one is under PD_Design and the other power domain is defined by taking the elements A1 and A2. While writing its command, an on state, off state along with input and output ports should be specified.[3]

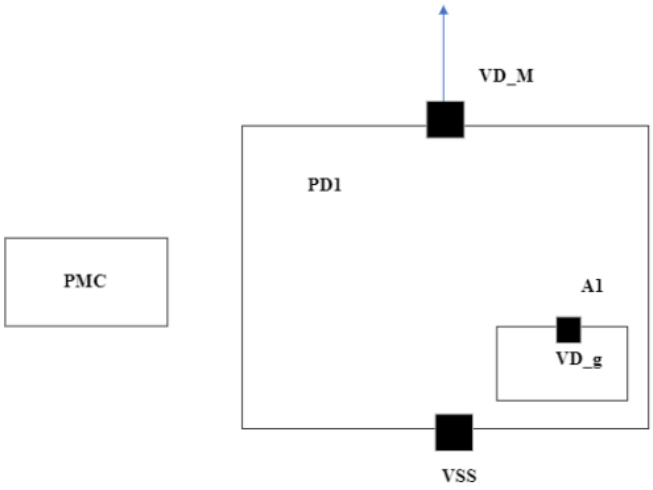

Fig 5:- Interdomain switch connection

If the interdomain connection is to be done a power management controller is needed, there are two nets VD_M and VD_g and if one signal is to be transported to another then a power switch is to be needed. An enable signal is needed to transfer VD_M to VD_g. When PG_EN =1 ,VD_g = VDD_M (ON); otherwise, VD_g = (OFF)

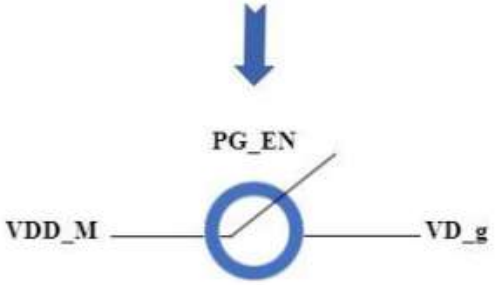

Fig 6:- Power Switch

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E. Power State Table

The arrangement of power supplies will be done using a power domain and defining supply net and port. Now a set of power patterns and combinations is required to tell which voltage combinations are valid and which are not. It is a very important component of the power intent file as all other commands are useless if this combination is not known. It is usually written in the form of a table where ports and power states are represented along with allowed voltages. There are many problems that are faced during static analysis like power states which are not legal or insufficient. Hence, they help in increasing efficiency and reduce the risk of failure of the power and verification process. All this is done using PST to perform analysis. The syntax for writing PST includes adding a port state and the creating table out of it.[12]

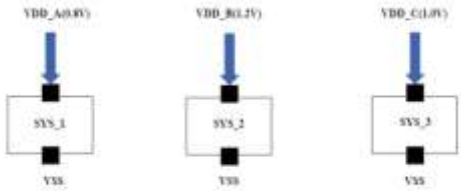

Fig 7:- Power Domains for PST

Three different systems are shown which represent three different components of the same power domain. The supplies along with the permittable voltage levels are as shown. A combination table is created which shows which values of voltages are allowed and at which valuesthe domains will be either switched on or off. While writing a UPF file, as power domain acts as the base, PST adds a structure to it along with allowed numerical values. The power domains are connected to VSS on the other side.[3]

Domain State	SYS_1	SYS_2	SYS_3
ALL_OFF	A_OFF	B_OFF	C_OFF
VOL_1	A_ON	B_OFF	C_OFF
VOL_2	A_ON	B_ON	C_OFF
ALL_ON	A_ON	B_ON	C_ON

Table 1:- Power State Table

The following table can be used to write the UPF file for the given design in such a manner that first ofall the states will be added by using add_port_state command. Then adding PST table withthe specified voltage levels and hence creating a PST.

```
add_port_state VDD_A -state {A_ON 0.8} -state {A_OFF OFF}
add_port_state VDD_B -state {B_ON 1.2} -state {B_OFF OFF}
add_port_state VDD_C -state {C_ON 1.0} -state {C_OFF OFF}
create PST T_PST supplies {A_ON B_ON C_ON}
add_pst_state ALL_OFF -pst T_PST -state {A_OFF B_OFF C_OFF}
```

The commands can be continued further according to the PST table, it represents a general format of commands used to create a PST table.PST adds a structure to UPF file.[12]

F. Level Shifter

When signals are crossing from one domain to the other usually the two power domains are not bound to be at the same voltage level which would otherwise lead to an indeterministic value, so a level shifter is a prime requirement. If the voltage levels of two power domains are different then a level shifter is required that either up shifts or down shifts the value according to the requirement. It is a very important cell as without this cell an indeterministic value can occur which can hamper the functionality of the design. At the same time it should be made sure that the level shifter gets proper supply from both ends so that it does not stop working. To define a level shifter, a name is required, in which domain and output or input side to which level shifter is to be applied and

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location is usually specified as self, it can be fanout, parent etc.[2]

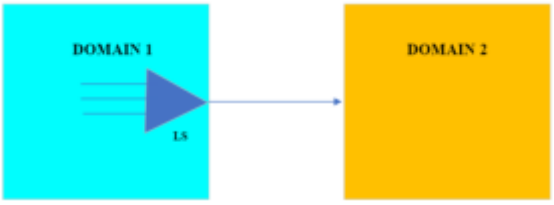

Fig 8:- Level Shifter

Fig 9:- Signal Mismatch

G. Isolation Cell

As the name suggests this cell is used for isolation purposes. Whenever one domain is shutting off due to the functionality of the design and the other one is on then this problem arises and an isolation cell is required. One domain shuts and if other is working then an unknown value floats in the circuit which can even lead to serious loss. An isolation cell fixes or clamps the value to either 0/1/latch along with its location and where it applies. Power domain 1 is off and 2 is on. The basic functioning of an isolation cell is that it consists of an input, an enable signal, and output. If enable signal is zero then input is not translated to output otherwise input is mapped as it is to output.[13]

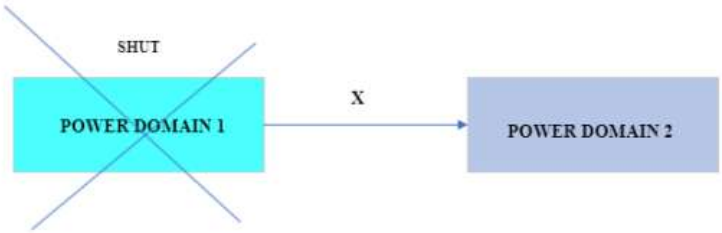

Fig 10:-Domain shut down

If EN = 0, input is not mapped to output.
If EN = 1, input is mapped to output.

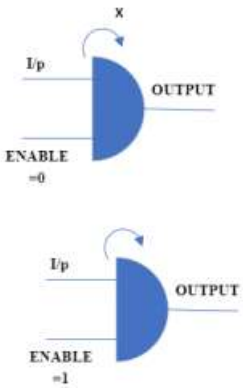

Fig 11:- Isolation Cell

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H. Retention Cells

There can be an instance if the primary power shuts down so the state which was held previously might not be retained, such a cell which is used to hold on to a state is known as retention cell as it is clear by the name itself. It usually takes more time as well as power resources to return back toa state if by chance that state is lost due to abrupt shut down also system can become unstable and unknown values can start occuring due to indeterministic state entering the system for which retention cell is employed.[7]

III. VC LP FLOW

Semiconductors have become very important for modern-day devices which demand higher performance and flexibility in terms of integration and growth. Many advances have been made inthis field recently like improved versions of phones and laptops have become very common and portable. These devices have one basic component which is a battery. The complex structures anddesigns have impacted the functionality of these systems in terms of improving performance. Power is the most critical factor which is required to make the device's performance very good.So, a universally accepted format named UPF which is reusable came into the picture which needs tobe run on this software by Synopsys called VCLP. It is a verification solution where various toolswork effortlessly to run the flow. Optimization and step-by-step iterating the design along with debugging is done using this software.[9]

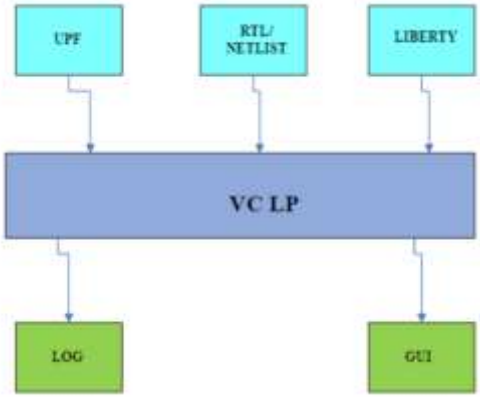

Fig 12:- VC LP Flow

IV. VC LP MESSAGES

Messages are an important communication medium between the tool and the user to find out about the current scenario of the design and its status. VC LP tool shows the messages in a combination of three keywords separated by underscores. First word depicts an electrical family, the second word depicts object having a problem and the third represents the existing problem. The first word can contain names of special cells and the second word can contain components of UPF like net, instance, or a strategy. The third word will focus on the problem which can be an improper placement of a cell or a missing cell etc. There are a total of eight combinations possible for the first keyword and many options available for the second keyword. The third keyword contains the problem and hence several combinations are possible for the third word as well. An example of a message can be ISO_STATE_MISSING which represents that an isolation cell has a power state which is missing in the design definition. By using only three keywords it becomes very simple to understand these messages.[11]

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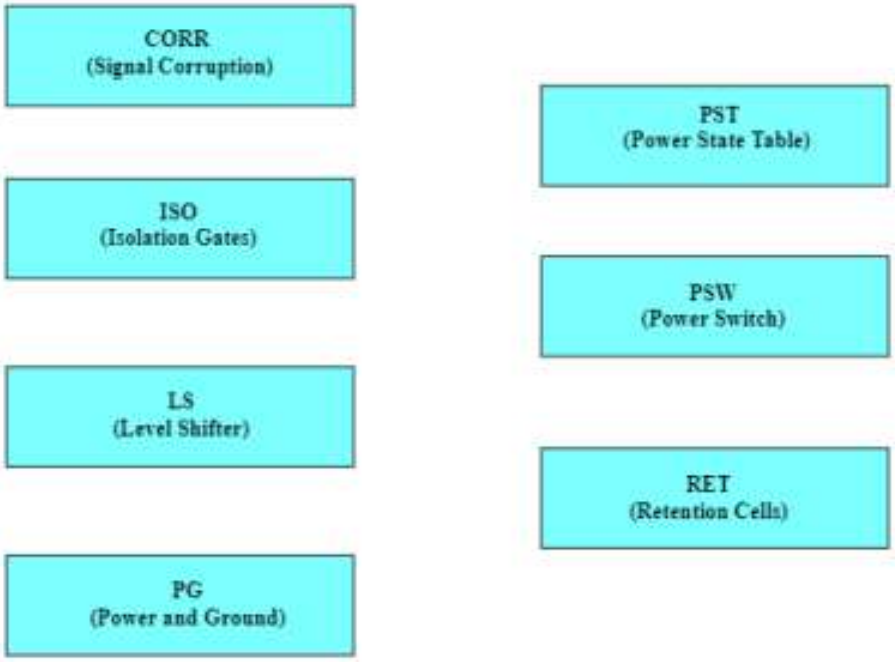

Fig 13:- Electrical families

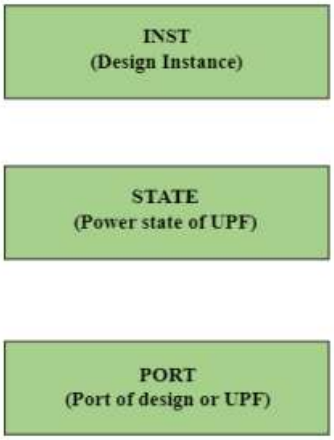

Fig 14 :- Object

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Fig 15:- Problem

V. VIOLATIONS

It is expected that a design should have very minimum or no violations but for a design in its initial stage tool might find a few errors and usage of the -verbose command can tell the details of received violations. There might be many reasons for huge errors, some problems can be there with the design specification or setup of the tool. So just by mere accident, many messages can appear, the beauty of this tool is that it only displays the first hundred messages of every tag giving flexibility of commands to display all the messages as well. Report_violations command can be used to get the summary.[7]

There might be many instances where tools might keep similar messages together in that case violations are compressed. Some rules have already been designed for such groupings by the tool, all this process works automatically as after deeply studying these violations a set of groups have been formed under which these violations could be grouped. As an example, two messages which contain problems like strategy missing and instance missing in case of an isolation cell, can be grouped as they both depict that an isolation cell is missing between the power domains. The question mark indicates a missing isolation cell.[8]

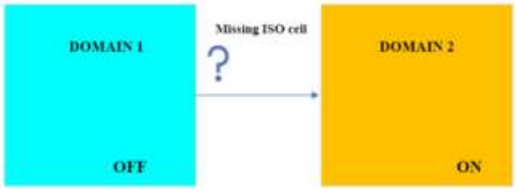

Fig 16:- Violation Compression

VI. RESULTS AND DISCUSSIONS

The industry is moving towards automation as compared to manual processing of work, UPF syntax and rules have already been defined but while dealing with several thousand supplies at the same time, automation comes into picture. It simplifies the script writing process and hence helps in saving time for the user. A series of activities done as a part of the internship majorly revolves around UPF. A basic UPF file requires writing a certain set of commands to be written repetitively like creating power domains, sets and

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nets. Such commands can take a lot of time when there are millions of power supplies available along with hundreds of domains. The automation was done using Python and Tcl scripting language. The automation of creating power domains and supply ports and nets is depicted. This automation involves an excel sheet that contains information about the names of power domains, supply nets, and ports specified in the form of sheets. The script is written in Python language using the Pandas library. A text file will be the output of this code which would write the UPF commands automatically in accordance with the excel sheet. Syntax of a UPF script is shown which picks values from the excel file already made manually by the user.[5]

	A	B	C
1	**Supply Name**	**Direction**	**Supply net**
2	VDD_A	IN	VDD_A
3	VDD_AB	OUT	VDD_AB
4	VDT	IN	VDT
5	JKU	IN	JKU
6	VLX	IN	VLX

	A	B	C	D	E
1	**Supply Set Name**	**Power**	**Ground**	**nwell**	**pwell**
2	SS1	VDD1	VSS1	VDD1	VSS1
3	SS2	VDD2	VSS2	VDD2	VSS2
4	SS3	VDD3	VSS3	VDD3	VSS3

Fig 17:- Excel sheet containing supply set and supply net information

This is the python code for the automation of UPF script.

```
import csv
import pandas as pd
import os

data = pd.read_excel("test.xlsx", sheet_name="Sheet1")
data = data.to_csv(r'upf.csv', header=False)

with open('upf.csv', 'r') as file:
    reader = csv.reader(file)
    with open('upf1.txt', 'w') as file1:
        for line in reader:
            file1.writelines("\n")
            file1.writelines("create_supply_port    " + line[1] + "   -direction  " + line[2])
            file1.writelines("\n")
            file1.writelines("create_supply_net     " + line[3])
            file1.writelines("\n")
            file1.writelines("connect_supply_net    " + line[3] + "   -ports      " + line[1])
            file1.writelines("\n")

data = pd.read_excel("test.xlsx", sheet_name="Sheet2")
data = data.to_csv(r'upf2.csv', header=False)

with open('upf2.csv', 'r') as file:
    reader = csv.reader(file)
    with open('upf2.txt', 'w') as file1:
        for line in reader:
            file1.writelines("\n")
            file1.writelines(
                "create_supply_set " + line[1] + "     -function  {power  " + line[2] + "}" +
                "     -function  {ground  " + line[3] + "}" +
                "     -function  {nwell  " + line[4] + "}" +
                "     -function  {pwell  " + line[5] + "}")
            file1.writelines("\n")
```

```
with open('upf1.txt', 'r') as file1:
    content1 = file1.read()

with open('upf2.txt', 'r') as file2:
    content2 = file2.read()

# Concatenate the contents of the two files
concatenated_content = content1 + ["\n\n"] + content2

with open('supply.txt', 'w') as output_file:
    output_file.write(concatenated_content)
os.remove("upf1.txt")
os.remove("upf2.txt")
os.remove("upf2.csv")
os.remove("upf.csv")
```

Fig 18:- Snapshot of python code

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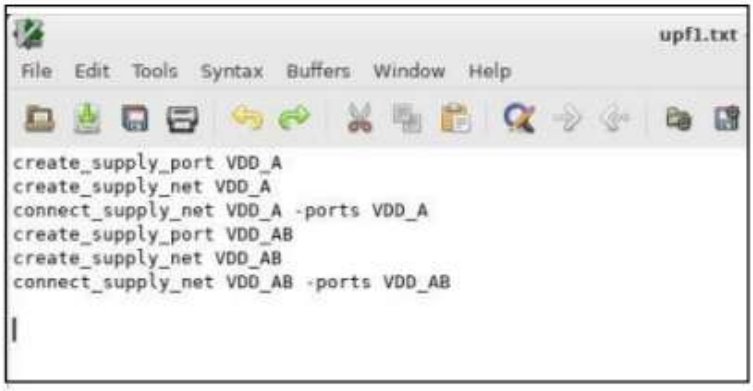


```
create_supply_set SS1 -function {power VDD1 }
                      -function {ground VSS1 }
                      -function{nwell VDD1 }
                      -function {pwell VSS1}
create_supply_set SS2 -function {power VDD2 }
                      -function {ground VSS2 }
                      -function{nwell VDD2 }
                      -function {pwell VSS2}
```

Fig 19:- Automation results

This is the format of UPF file is written below,

/## create supply nets and ports ## #######
create_supply_net VD_A
create_supply_portVD_A -direction in
connect_supply_net VD_A -ports VD_A
create_supply_net VD_B
create_supply_port VD_B -direction in
connect_supply_net VD_B - ports VD_B
create_supply_net VD_C
create_supply_port VD_C-direction in
connect_supply_net VD_C -ports VD_C
create supply nets create_supply_set AS_A \
-function {power VD_B} \ -function {ground ground} \ -function {nwell VD_C}
-function {pwell ground}
create_supply_set BS_B \
-function {power VD_C} \
-function {ground gnd} \
-function {nwell VD_C} \
-function {pwellgnd}
creating power domain create_power_domain PD_ABC -include_scope \
-supply {primary SS_VD_B_GND} \ -available_supplies {SS_VD_C_GND}
-ports "${memory}/VD_D"connect_supply_netgnd
-ports "${memory}/VS_ S
}
##PST
########################
add_power_state -supply ss_vdd_varm_gnd \
-state NOM
{
-supply_expr {power == {ON X} && ground == {ON X} &&nwell == {FULL_on X} &&pwell == {FULL_on X}}} \
-state HIGH {-supply_expr {power == {ON X} && ground == {ON X} &&nwell == {FULL_on X} &&pwell == {FULL_on X}}}

This UPF is integrated into top after which with the help of the placement and routing team trials were conducted based on the supply being given in the UPF. In VC LP runs to resolve some errors creation of dummy nets was done. A comparison of these runs with the actual runs was done to understand the difference between the two and to check whether the errors are resolved or not. A total of three trials were done using the VC LP tool and the number of errors were checked. The file named Design_In_Out_Variables contains the reference netlist and UPF and sets the variable defined only in the reference flow. In the first run, if we suppose a hundred violations are coming after analysis half of the violations are skipped or waived by the tool, now if in the second iteration

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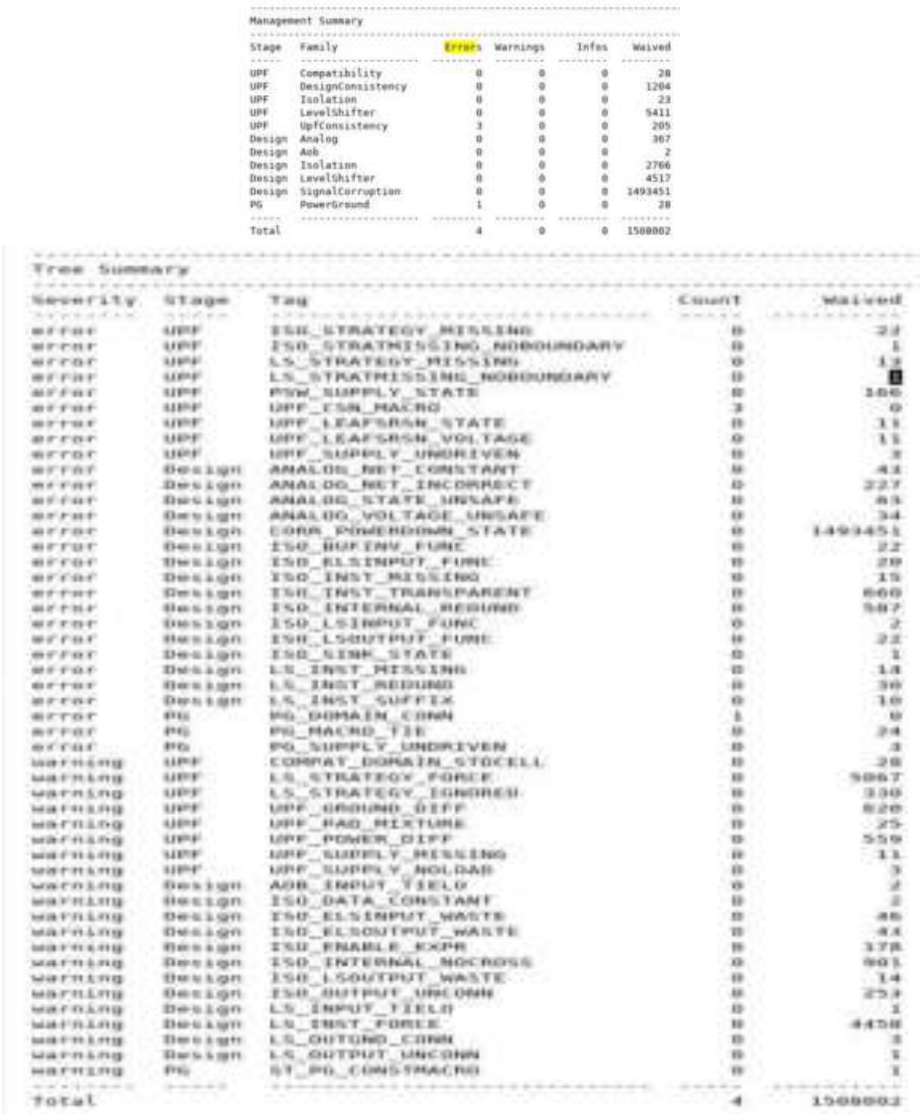
more than a hundred violations come now those fifty waived-off sessions will not interfere with these violations. The first trial is that of a golden UPF and a check summary report showing the number of errors. This is to be compared and increased at every stage of the design flow. The first trial shows the management summary and in detail tree summary which shows the stage, family and number of errors waived by the tool which will not disturb the design in further iterations.[6]



Management Summary

Stage	Family	Errors	Warnings	Infos	Waived
UPF	Compatibility	0	0	0	28
UPF	DesignConsistency	0	0	0	1204
UPF	Isolation	0	0	0	23
UPF	LevelShifter	0	0	0	5411
UPF	UpfConsistency	3	0	0	205
Design	Analog	0	0	0	367
Design	Aob	0	0	0	2
Design	Isolation	0	0	0	2766
Design	LevelShifter	0	0	0	4517
Design	SignalCorruption	0	0	0	1493451
PG	PowerGround	1	0	0	28
Total		4	0	0	1508002

Tree Summary

Severity	Stage	Tag	Count	Waived
error	UPF	ISO_STRATEGY_MISSING	0	22
error	UPF	ISO_STRATMISSING_NOBOUNDARY	0	1
error	UPF	LS_STRATEGY_MISSING	0	13
error	UPF	LS_STRATMISSING_NOBOUNDARY	0	1
error	UPF	PSW_SUPPLY_STATE	0	166
error	UPF	UPF_CSN_MACRO	3	0
error	UPF	UPF_LEAFSRSN_STATE	0	11
error	UPF	UPF_LEAFSRSN_VOLTAGE	0	11
error	UPF	UPF_SUPPLY_UNDRIVEN	0	3
error	Design	ANALOG_NET_CONSTANT	0	41
error	Design	ANALOG_NET_INCORRECT	0	227
error	Design	ANALOG_STATE_UNSAFE	0	65
error	Design	ANALOG_VOLTAGE_UNSAFE	0	34
error	Design	CORR_POWERDOWN_STATE	0	1493451
error	Design	ISO_BUFINV_FUNC	0	22
error	Design	ISO_ELSINPUT_FUNC	0	28
error	Design	ISO_INST_MISSING	0	15
error	Design	ISO_INST_TRANSPARENT	0	660
error	Design	ISO_INTERNAL_REQUND	0	587
error	Design	ISO_LSINPUT_FUNC	0	2
error	Design	ISO_LSOUTPUT_FUNC	0	22
error	Design	ISO_SINK_STATE	0	1
error	Design	LS_INST_MISSING	0	13
error	Design	LS_INST_REQUND	0	36
error	Design	LS_INST_SUFFIX	0	16
error	PG	PG_DOMAIN_CONN	1	0
error	PG	PG_MACRO_TIE	0	24
error	PG	PG_SUPPLY_UNDRIVEN	0	3
warning	UPF	COMPAT_DOMAIN_STDCELL	0	28
warning	UPF	LS_STRATEGY_FORCE	0	5067
warning	UPF	LS_STRATEGY_IGNORED	0	330
warning	UPF	UPF_GROUND_DIFF	0	620
warning	UPF	UPF_PAD_MIXTURE	0	25
warning	UPF	UPF_POWER_DIFF	0	559
warning	UPF	UPF_SUPPLY_MISSING	0	11
warning	UPF	UPF_SUPPLY_NOLOAD	0	3
warning	Design	AOB_INPUT_FIELD	0	2
warning	Design	ISO_DATA_CONSTANT	0	1
warning	Design	ISO_ELSINPUT_WASTE	0	46
warning	Design	ISO_ELSOUTPUT_WASTE	0	44
warning	Design	ISO_ENABLE_EXPR	0	178
warning	Design	ISO_INTERNAL_NOCROSS	0	901
warning	Design	ISO_LSOUTPUT_WASTE	0	14
warning	Design	ISO_OUTPUT_UNCONN	0	253
warning	Design	LS_INPUT_FIELD	0	1
warning	Design	LS_INST_FORCE	0	4458
warning	Design	LS_OUTGND_CONN	0	3
warning	Design	LS_OUTPUT_UNCONN	0	1
warning	PG	GT_PG_CONSTMACRO	0	1
Total			4	1508002

Fig 20 :- Snapshot of summary of trial 1

Both management and tree summary is shown in the figures.

The second trial was done by commenting one supply net to check its impact on the number of violations and errors coming and the number of errors waived off was reduced by one in the management and tree summary. The same warning of connect_supply_net missing with different codes is shown in the figure which were encountered in the first trial named UPF_CSN_MACRO.

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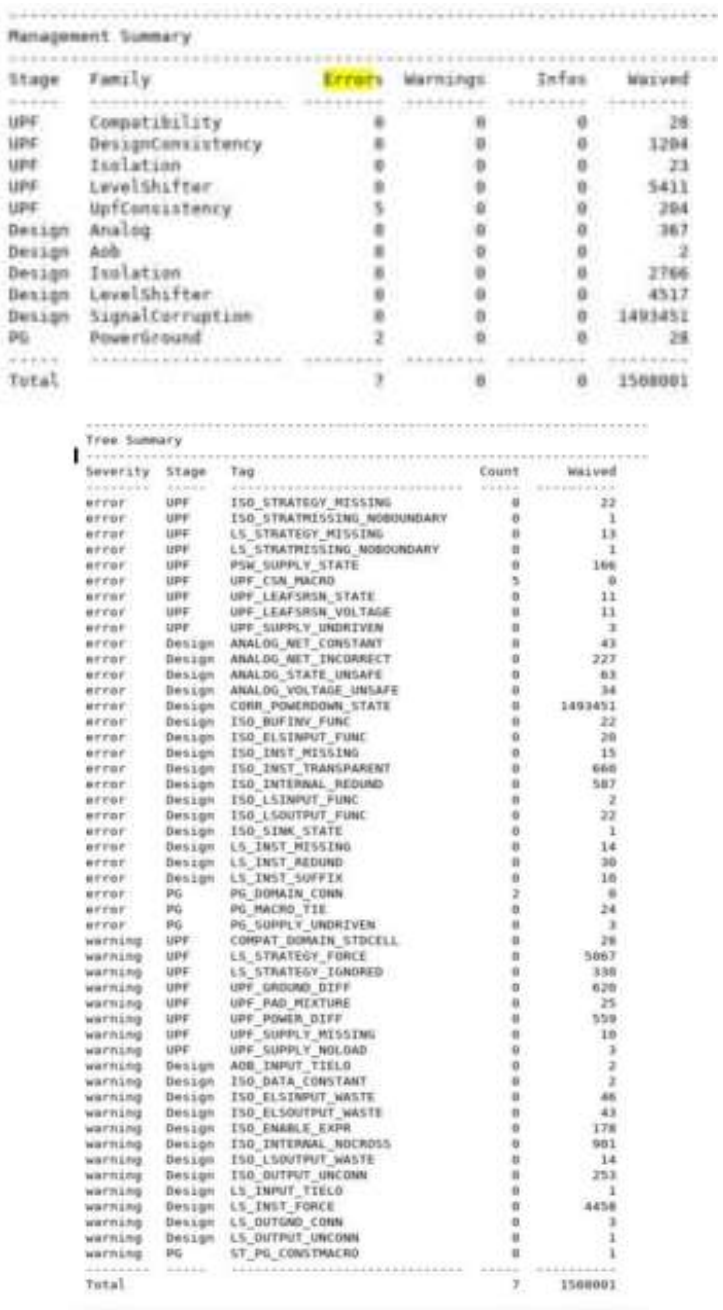

Management Summary

Stage	Family	Errors	Warnings	Infos	Waived
UPF	Compatibility	0	0	0	28
UPF	DesignConsistency	0	0	0	1204
UPF	Isolation	0	0	0	23
UPF	LevelShifter	0	0	0	5411
UPF	UpfConsistency	5	0	0	204
Design	Analog	0	0	0	367
Design	Aob	0	0	0	2
Design	Isolation	0	0	0	2766
Design	LevelShifter	0	0	0	4517
Design	SignalCorruptinn	0	0	0	1493451
PG	PowerGround	2	0	0	28
Total		7	0	0	1508001

Tree Summary

Severity	Stage	Tag	Count	Waived
error	UPF	ISO_STRATEGY_MISSING	0	22
error	UPF	ISO_STRATMISSING_NOBOUNDARY	0	1
error	UPF	LS_STRATEGY_MISSING	0	13
error	UPF	LS_STRATMISSING_NOBOUNDARY	0	1
error	UPF	PSW_SUPPLY_STATE	0	166
error	UPF	UPF_CSN_MACRO	5	0
error	UPF	UPF_LEAFSRSN_STATE	0	11
error	UPF	UPF_LEAFSRSN_VOLTAGE	0	11
error	UPF	UPF_SUPPLY_UNDRIVEN	0	3
error	Design	ANALOG_NET_CONSTANT	0	43
error	Design	ANALOG_NET_INCORRECT	0	227
error	Design	ANALOG_STATE_UNSAFE	0	63
error	Design	ANALOG_VOLTAGE_UNSAFE	0	34
error	Design	CORR_POWERDOWN_STATE	0	1493451
error	Design	ISO_BUFINV_FUNC	0	22
error	Design	ISO_ELSINPUT_FUNC	0	20
error	Design	ISO_INST_MISSING	0	15
error	Design	ISO_INST_TRANSPARENT	0	666
error	Design	ISO_INTERNAL_REDUND	0	587
error	Design	ISO_LSINPUT_FUNC	0	2
error	Design	ISO_LSOUTPUT_FUNC	0	22
error	Design	ISO_SINK_STATE	0	1
error	Design	LS_INST_MISSING	0	14
error	Design	LS_INST_REDUND	0	30
error	Design	LS_INST_SUFFIX	0	10
error	PG	PG_DOMAIN_CONN	2	0
error	PG	PG_MACRO_TIE	0	24
error	PG	PG_SUPPLY_UNDRIVEN	0	3
warning	UPF	COMPAT_DOMAIN_STDCELL	0	28
warning	UPF	LS_STRATEGY_FORCE	0	5067
warning	UPF	LS_STRATEGY_IGNORED	0	330
warning	UPF	UPF_GROUND_DIFF	0	620
warning	UPF	UPF_PAD_MIXTURE	0	25
warning	UPF	UPF_POWER_DIFF	0	559
warning	UPF	UPF_SUPPLY_MISSING	0	10
warning	UPF	UPF_SUPPLY_NOLOAD	0	3
warning	Design	AOB_INPUT_TIELO	0	2
warning	Design	ISO_DATA_CONSTANT	0	2
warning	Design	ISO_ELSINPUT_WASTE	0	46
warning	Design	ISO_ELSOUTPUT_WASTE	0	43
warning	Design	ISO_ENABLE_EXPR	0	178
warning	Design	ISO_INTERNAL_NOCROSS	0	901
warning	Design	ISO_LSOUTPUT_WASTE	0	14
warning	Design	ISO_OUTPUT_UNCONN	0	253
warning	Design	LS_INPUT_TIELO	0	1
warning	Design	LS_INST_FORCE	0	4458
warning	Design	LS_OUTGND_CONN	0	3
warning	Design	LS_OUTPUT_UNCONN	0	1
warning	PG	ST_PG_CONSTMACRO	0	1
Total			7	1508001

Fig 21 :- Snapshot of summary of trial 2

In the third trial, same thing was repeated again, including one more error of PG_DOMAIN_CONN where the pin or supply is not getting matched, again a very common error, a dummy supply was commented to check its impact on the number of errors waived by the tool. It was observed that it waived off one less error as compared to the previous trial.

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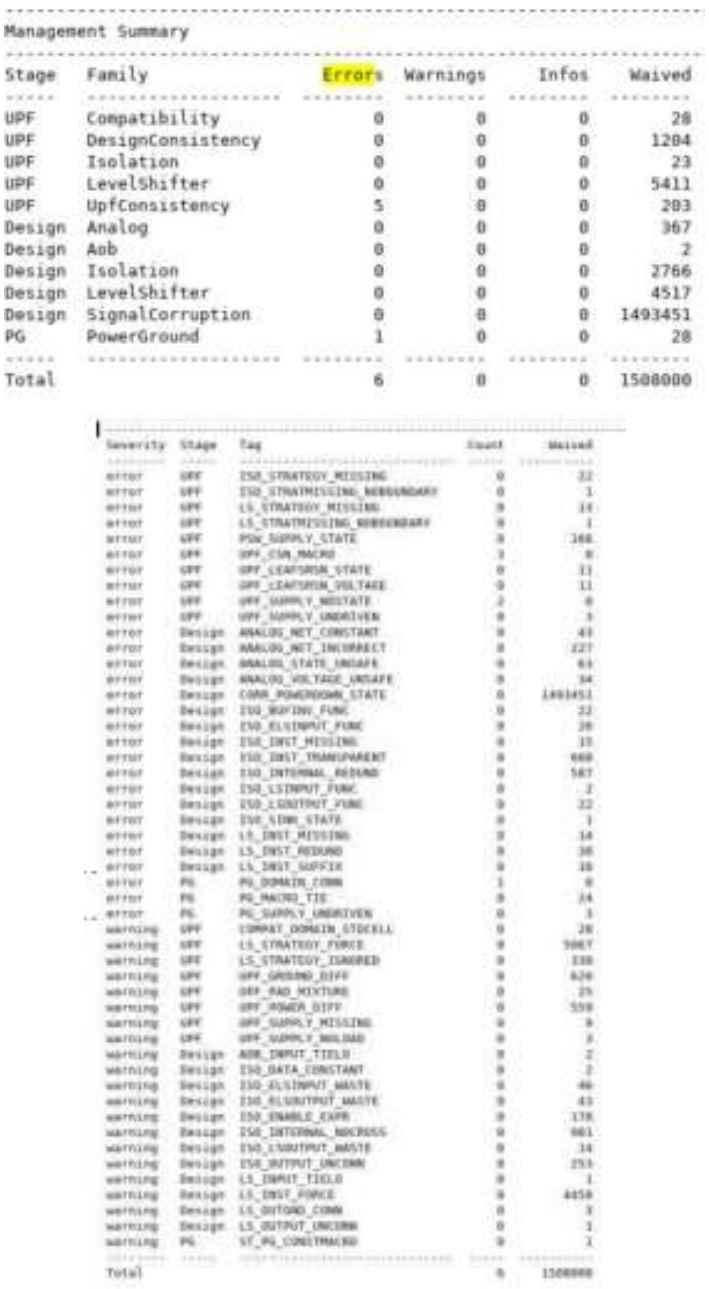

Management Summary

Stage	Family	Errors	Warnings	Infos	Waived
UPF	Compatibility	0	0	0	28
UPF	DesignConsistency	0	0	0	1204
UPF	Isolation	0	0	0	23
UPF	LevelShifter	0	0	0	5411
UPF	UpfConsistency	5	0	0	203
Design	Analog	0	0	0	367
Design	Aob	0	0	0	2
Design	Isolation	0	0	0	2766
Design	LevelShifter	0	0	0	4517
Design	SignalCorruption	0	0	0	1493451
PG	PowerGround	1	0	0	28
Total		6	0	0	1508000

Fig 22 :- Snapshot of summary of trial 3

The number of errors waived is increasing as commenting of supply nets is done which shows the importance of creating dummy nets. Theseviolations are very important even at later stages of design flow.

VII. CONCLUSION

The purpose of this work was to understand the UPF files and learn about techniques to save power in a complex design. As every design goes through the design flow incorporating a power file at every stage ensures that the power is well defined and design is well aware about the power and its impact can be such that it can help in low power devices. The work concludes with three trials showing the wavering of a huge number of errors and shows the impact of dummy nets on the errors and hence design.

Only RTL simulation alone cannot contribute to power saving and verification, integration of both files is needed to finally simulate the design. The understanding of

violations and errors helped in understanding what is happening at ground level which in turn leaves room for any further designchallenges that might be faced in future. Overall, a UPF file is very compact and can be easily altered and integrated at design flow steps. Without a UPF file no new design in the backend can begin as it is the initial as well as the final stage of product development and flow. In our day-to-day life cannot be imagined without low-power devices and this demand is increasing every day.

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